Document Title

128K x8 bit Low Power CMOS Static RAM

Revision History

Revision No.	History	Draft Date	Remark
0.0	Initial draft	November 22, 1995	Design target
0.1	First revision - Seperate read and write at I_{CC}, I_{CC1} $I_{CC} = I_{CC1} \rightarrow$ Read : 15mA, Write : 35mA	April 15, 1996	Preliminary
1.0	Finalized - Add 70ns speed bin for commercial product and 85ns speed bin for industrial.	September 5, 1996	Final
2.0	Revised - Improved operating current Add typical value. I_{CC} Read : 15mA $\rightarrow$ 10mA(Remove write current) I_{CC2} : 90mA $\rightarrow$ 60mA - Speed bin change Remove 45ns from commercial part Remove 55ns and 100ns from industrial part.	November 5, 1997	Final

128K x8 bit Low Power CMOS Static RAM

FEATURES

- Process Technology: TFT
- Organization: 128K x8
- Power Supply Voltage: 4.5~5.5V
- Low Data Retention Voltage: 2V(Min)
- Three state output and TTL Compatible
- Package Type: 32-DIP-600, 32-SOP-525, 32-TSOP1-0820F/R

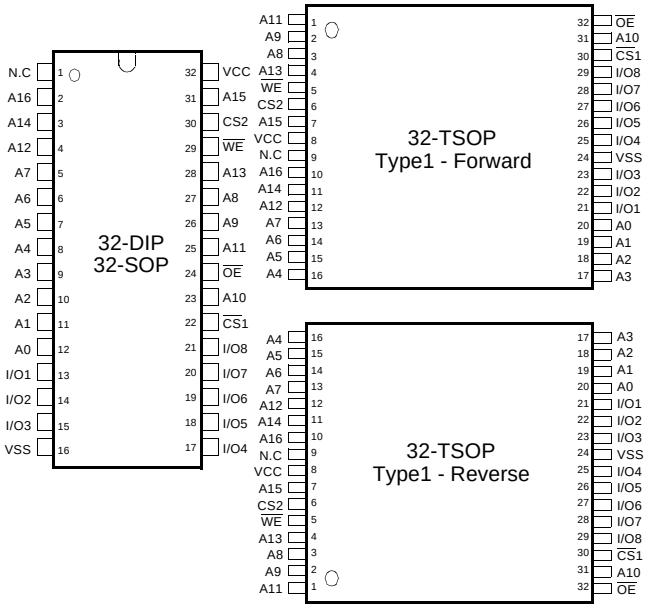
GENERAL DESCRIPTION

The KM681000C families are fabricated by SAMSUNG′s advanced CMOS process technology. The families support various operating temperature ranges and have various package types for user flexibility of system design. The families also support low data retention voltage for battery back-up operation with low data retention current.

PRODUCT FAMILY

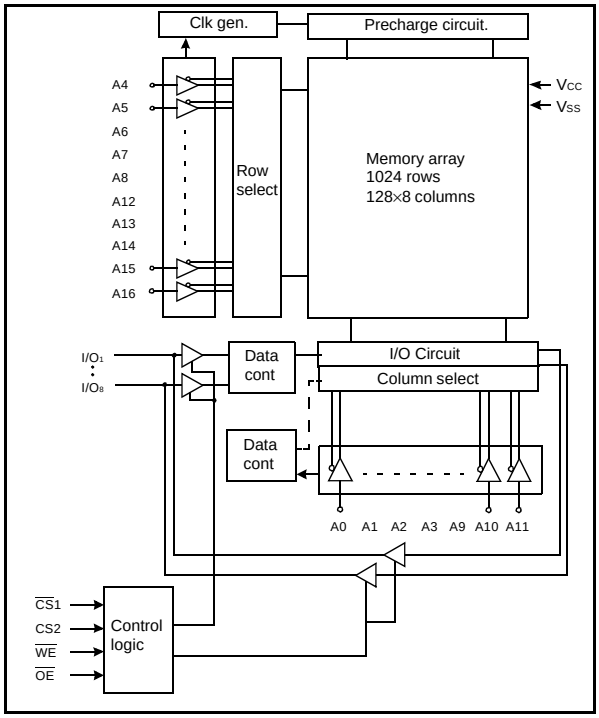
Product Family	Operating Temperature	Vcc Range	Speed	Power Dissipation		PKG Type
				Standby (I_{SB1}, Max)	Operating (I_{CC2}, Max)	
KM681000CL KM681000CL-L	Commercial(0~70°C)	4.5~5.5V	55/70ns	50µA 10µA	60mA	32-DIP, 32-SOP 32-TSOP1-F/R
KM681000CLI KM681000CLI-L	Industrial(-40~85°C)		70ns	50µA 15µA		32-SOP 32-TSOP1-F/R

PIN DESCRIPTION



Name	Function	Name	Function
$\overline{CS_1}$,CS_2	Chip Select Inputs	I/O_1~I/O_8	Data Inputs/Out-
$\overline{OE}$	Output Enable	Vcc	Power
$\overline{WE}$	Write Enable	Vss	Ground
A_0~A_{16}	Address Inputs	N.C	No Connection

FUNCTIONAL BLOCK DIAGRAM



PRODUCT LIST

Commercial Temperature Products(0~70°C)		Industrial Temperature Products(-40~85°C)	
Part Name	**Function**	**Part Name**	**Function**
KM681000CLP-5	32-DIP, 55ns, L-pwr	KM681000CLGI-7	32-SOP, 70ns, L-pwr
KM681000CLP-7	32-DIP, 70ns, L-pwr	KM681000CLGI-7L	32-SOP, 70ns, LL-pwr
KM681000CLP-5L	32-DIP, 55ns, LL-pwr		
KM681000CLP-7L	32-DIP, 70ns, LL-pwr	KM681000CLTI-7L	32-TSOP1-F, 70ns, LL-pwr
KM681000CLG-5	32-SOP, 55ns, L-pwr	KM681000CLRI-7L	32-TSOP1-R, 70ns, LL-pwr
KM681000CLG-7	32-SOP, 70ns, L-pwr		
KM681000CLG-5L	32-SOP, 55ns, LL-pwr		
KM681000CLG-7L	32-SOP, 70ns, LL-pwr		
KM681000CLT-5L	32-TSOP1-F, 55ns, LL-pwr		
KM681000CLT-7L	32-TSOP1-F, 70ns, LL-pwr		
KM681000CLR-5L	32-TSOP1-R, 55ns, LL-pwr		
KM681000CLR-7L	32-TSOP1-R, 70ns, LL-pwr		

FUNCTIONAL DESCRIPTION

$\overline{CS_1}$	CS_2	$\overline{OE}$	$\overline{WE}$	I/O Pin	Mode	Power
H	X[1]	X[1]	X[1]	High-Z	Deselected	Standby
X[1]	L	X[1]	X[1]	High-Z	Deselected	Standby
L	H	H	H	High-Z	Output Disable	Active
L	H	L	H	Dout	Read	Active
L	H	X[1]	L	Din	Write	Active

1. X means don't care(Must be in high or low status.)

ABSOLUTE MAXIMUM RATINGS[1]

Item	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-0.5 to 7.0	V	-
Voltage on Vcc supply relative to Vss	V_{CC}	-0.5 to 7.0	V	-
Power Dissipation	P_D	1.0	W	-
Storage temperature	T_{STG}	-65 to 150	°C	-
Operating Temperature	T_A	0 to 70	°C	KM681000CL
		-40 to 85	°C	KM681000CLI
Soldering temperature and time	T_{SOLDER}	260°C, 10sec (Lead Only)	-	-

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS[1)]

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	Vcc	4.5	5.0	5.5	V
Ground	Vss	0	0	0	V
Input high voltage	V_{IH}	2.2	-	Vcc+0.5[2)]	V
Input low voltage	V_{IL}	-0.5[3)]	-	0.8	V

Note
1. Commercial Product : T_A=0 to 70°C and Industrial Product :T_A=-40 to 85°C, otherwise specified.
2. Overshoot : Vcc+3.0V for≤30ns pulse width.
3. Undershoot : -3.0V for≤30ns pulse width.
4. Overshoot and undershoot are sampled, not 100% tested.

CAPACITANCE[1)] (f=1MHz, T_A=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C_{IN}	V_{IN}=0V	-	6	pF
Input/Output capacitance	C_{IO}	V_{IO}=0V	-	8	pF

1. Capacitance is sampled not, 100% tested.

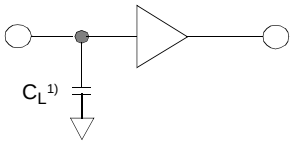
DC AND OPERATING CHARACTERISTICS

Item		Symbol	Test Conditions		Min	Typ	Max	Unit
Input leakage current		I_{LI}	V_{IN}=Vss to Vcc		-1	-	1	µA
Output leakage current		I_{LO}	$\overline{CS_1}$=V_{IH} or CS_2=V_{IL} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL}, V_{IO}=Vss to Vcc		-1	-	1	µA
Operating power supply current		I_{CC}	I_{IO}=0mA, $\overline{CS_1}$=V_{IL}, CS_2=V_{IH}, V_{IN}=V_{IH} or V_{IL}, Read		-	5	10	mA
Average operating current		I_{CC1}	Cycle time=1µs, 100% duty, I_{IO}=0mA, $\overline{CS_1}$≤0.2V, CS_2≥V_{CC}-0.2V, V_{IN}≤0.2V or V_{IN}≥V_{CC}-0.2V	Read	-	2	5	mA
				Write		20	35	
		I_{CC2}	Cycle time=Min, 100% duty, I_{IO}=0mA, $\overline{CS_1}$=V_{IL}, CS_2=V_{IH},V_{IN}=V_{IL} or V_{IH}		-	45	60	mA
Output low voltage		V_{OL}	I_{OL}=2.1mA		-	-	0.4	V
Output high voltage		V_{OH}	I_{OH}=-1.0mA		2.4	-	-	V
Standby Current(TTL)		I_{SB}	$\overline{CS_1}$=V_{IH}, CS_2=V_{IL}, Other input=V_{IL} or V_{IH}		-	-	3	mA
Standby Current (CMOS)	KM681000CL	I_{SB1}	$\overline{CS_1}$≥Vcc-0.2V, CS2≥Vcc-0.2V or CS_2≤0.2V Other input =0~Vcc	Low Power	-	1	50	µA
	KM681000CL-L			Low Low Power	-	0.3	10	
	KM681000CLI			Low power	-	1	50	
	KM681000CLI-L			Low Low Power	-	0.3	15	

AC OPERATING CONDITIONS

TEST CONDITIONS (Test Load and Test Input/Output Reference)

Input pulse level : 0.8 to 2.4V
Input rising and falling time : 5ns
Input and output reference voltage : 1.5V
Output load (See right) :C_L=100pF+1TTL



1. Including scope and jig capacitance

AC CHARACTERISTICS

Parameter List		Symbol	Speed Bins				Units
			55ns		70ns		
			Min	Max	Min	Max	
Read	Read cycle time	t_{RC}	55	-	70	-	ns
	Address access time	t_{AA}	-	55	-	70	ns
	Chip select to output	t_{CO1}, t_{CO2}	-	55	-	70	ns
	Output enable to valid output	t_{OE}	-	25	-	35	ns
	Chip select to low-Z output	t_{LZ}	10	-	10	-	ns
	Output enable to low-Z output	t_{OLZ}	5	-	5	-	ns
	Chip disable to high-Z output	t_{HZ}	0	20	0	25	ns
	Output disable to high-Z output	t_{OHZ}	0	20	0	25	ns
	Output hold from address change	t_{OH}	10	-	10	-	ns
Write	Write cycle time	t_{WC}	55	-	70	-	ns
	Chip select to end of write	t_{CW}	45	-	60	-	ns
	Address set-up time	t_{AS}	0	-	0	-	ns
	Address valid to end of write	t_{AW}	45	-	60	-	ns
	Write pulse width	t_{WP}	40	-	50	-	ns
	Write recovery time	t_{WR1},t_{WR2}	0	-	0	-	ns
	Write to output high-Z	t_{WHZ}	0	20	0	25	ns
	Data to write time overlap	t_{DW}	25	-	30	-	ns
	Data hold from write time	t_{DH}	0	-	0	-	ns
	End write to output low-Z	t_{OW}	5	-	5	-	ns

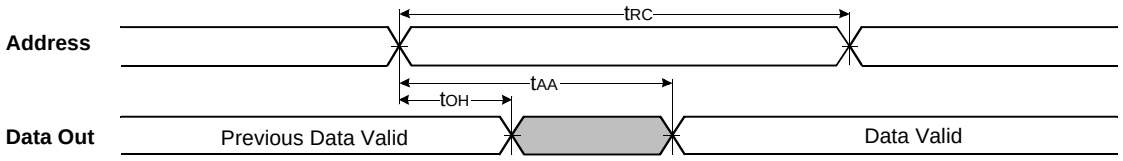
DATA RETENTION CHARACTERISTICS

Item	Symbol	Test Condition		Min	Typ	Max	Unit
Vcc for data retention	V_{DR}	$\overline{CS_1}$ 1)≥Vcc-0.2V, CS_2≥Vcc-0.2V or CS_2≤0.2V		2.0	-	5.5	V
Data retention current	I_{DR}	Vcc=3.0V, $\overline{CS_1}$≥Vcc-0.2V, CS2≥Vcc-0.2V or CS_2≤0.2V	KM681000CL	-	1	20	µA
			KM681000CL-L	-	1	10	
			KM681000CLI	-	-	25	
			KM681000CLI-L	-	-	10	
Data retention set-up	t_{SDR}	See data retention waveform		0	-	-	ms
Recovery time	t_{RDR}			5	-	-	

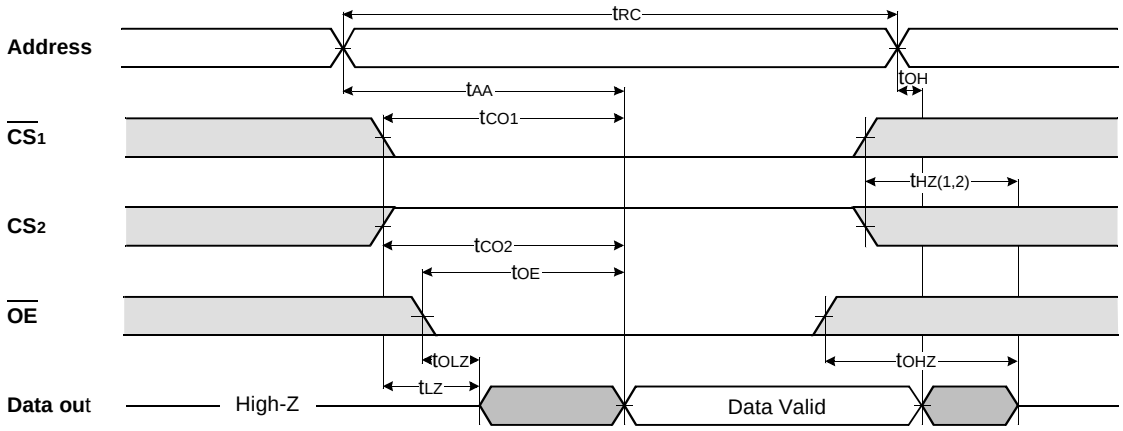
1. $\overline{CS_1}$≥Vcc-0.2v, CS_2≥Vcc-0.2V or CS_2≤0.2V

TIMMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled, $\overline{CS_1}$=$\overline{OE}$=V_{IL}, $\overline{WE}$=V_{IH})



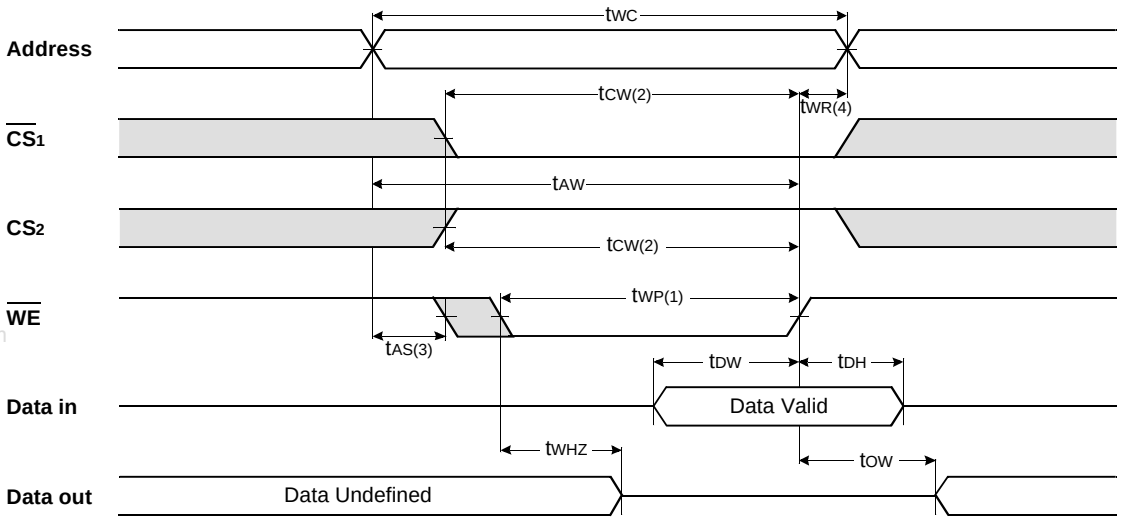
TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}$=V_{IH})



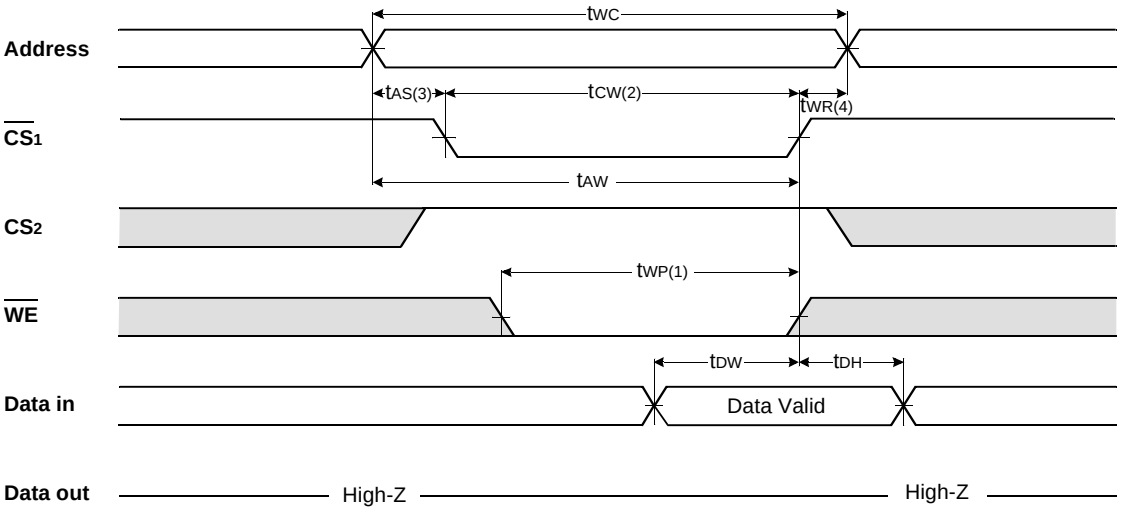
NOTES (READ CYCLE)

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, t_{HZ}(Max.) is less than t_{LZ}(Min.) both for a given device and from device to device interconnection.

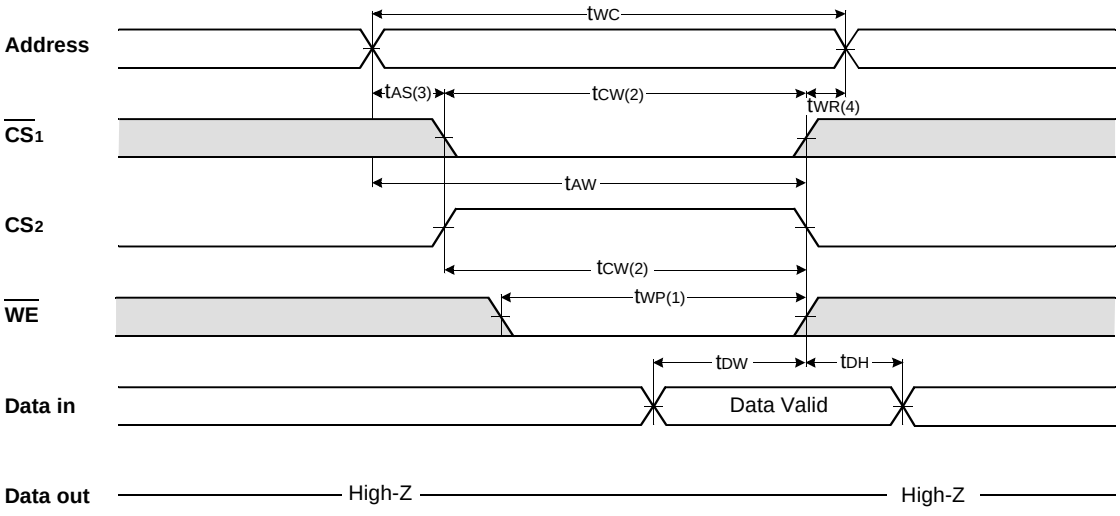
TIMING WAVEFORM OF WRITE CYCLE(1) ($\overline{WE}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{CS_1}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE(3) (CS_2 Controlled)

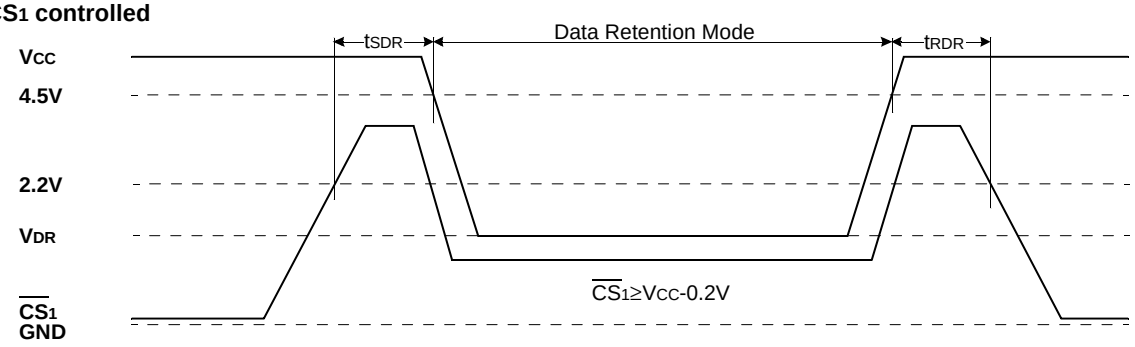


NOTES (WRITE CYCLE)

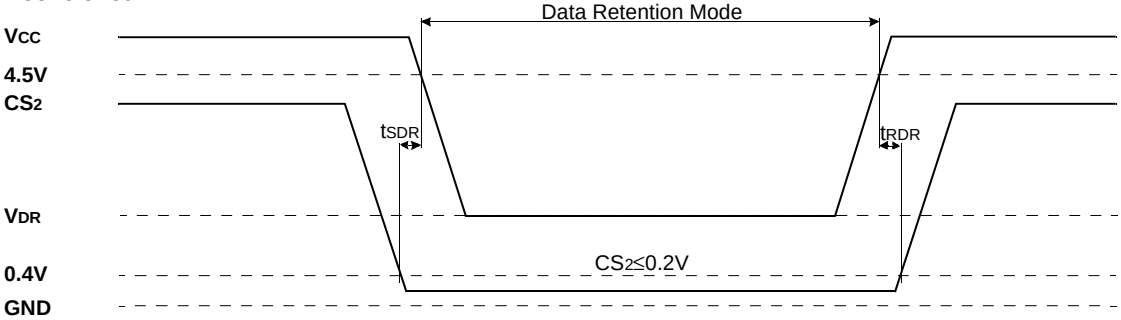
1. A write occurs during the overlap of a low $\overline{CS_1}$, a high CS_2 and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS_1}$ goes low, CS_2 going high and WE going low : A write end at the earliest transition among CS_1 going high, CS_2 going low and WE going high, t_{WP} is measured from the begining of write to the end of write.
2. t_{CW} is measured from the $\overline{CS_1}$ going low or CS_2 going high to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. $t_{WR(1)}$ applied in case a write ends as $\overline{CS_1}$ or $\overline{WE}$ going high $t_{WR(2)}$ applied in case a write ends as CS_2 going to low.

DATA RETENTION WAVE FORM

$\overline{CS_1}$ controlled



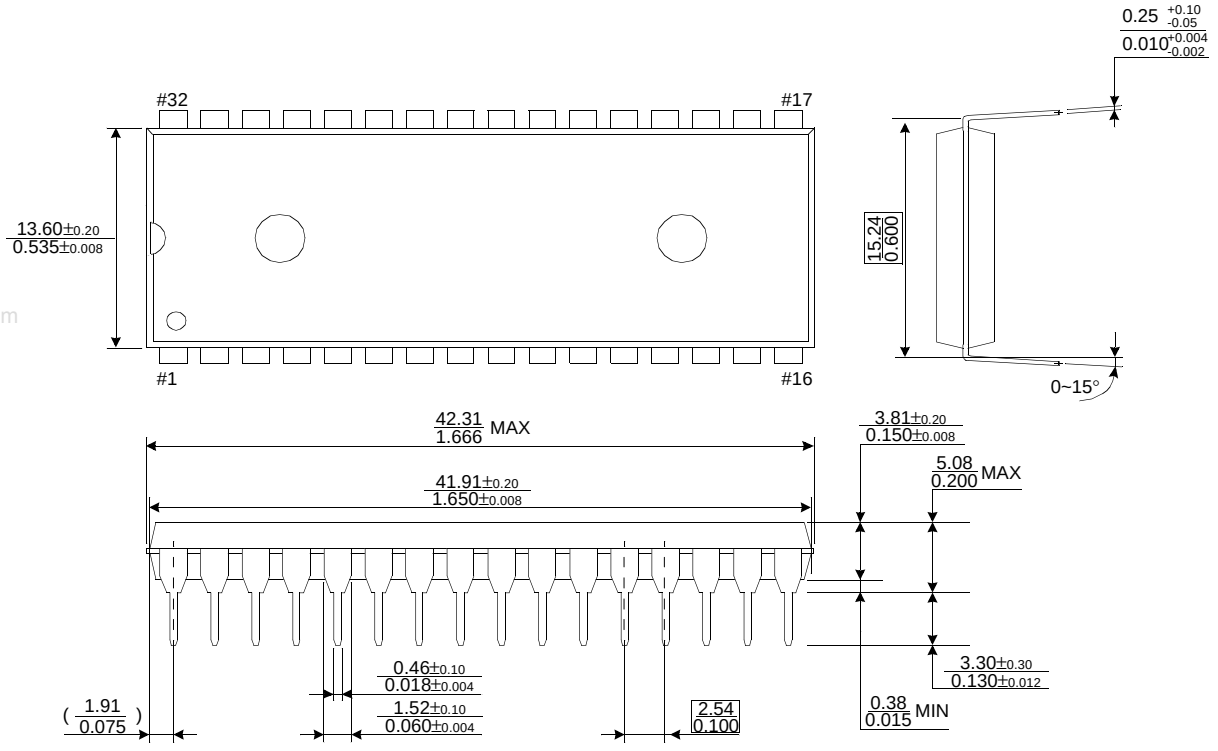
CS_2 controlled



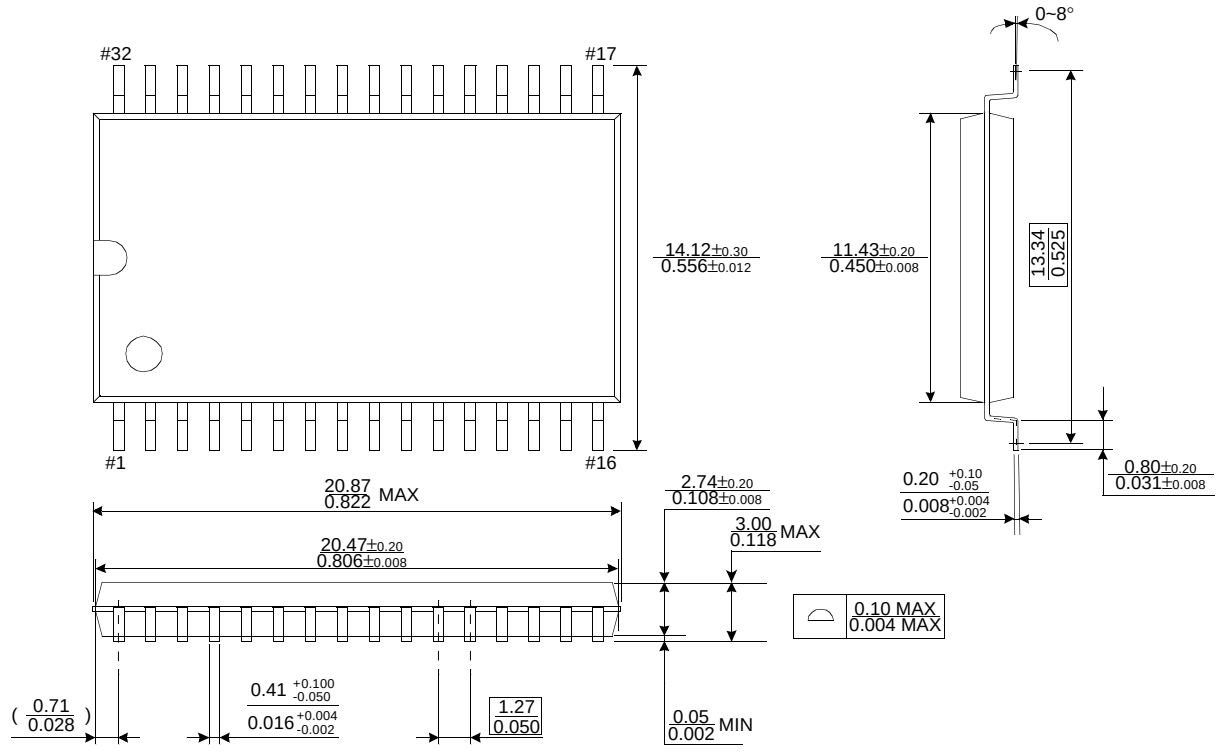
PACKAGE DIMENSIONS

Units: millimeter(inch)

32 DUAL INLINE PACKAGE (600mil)



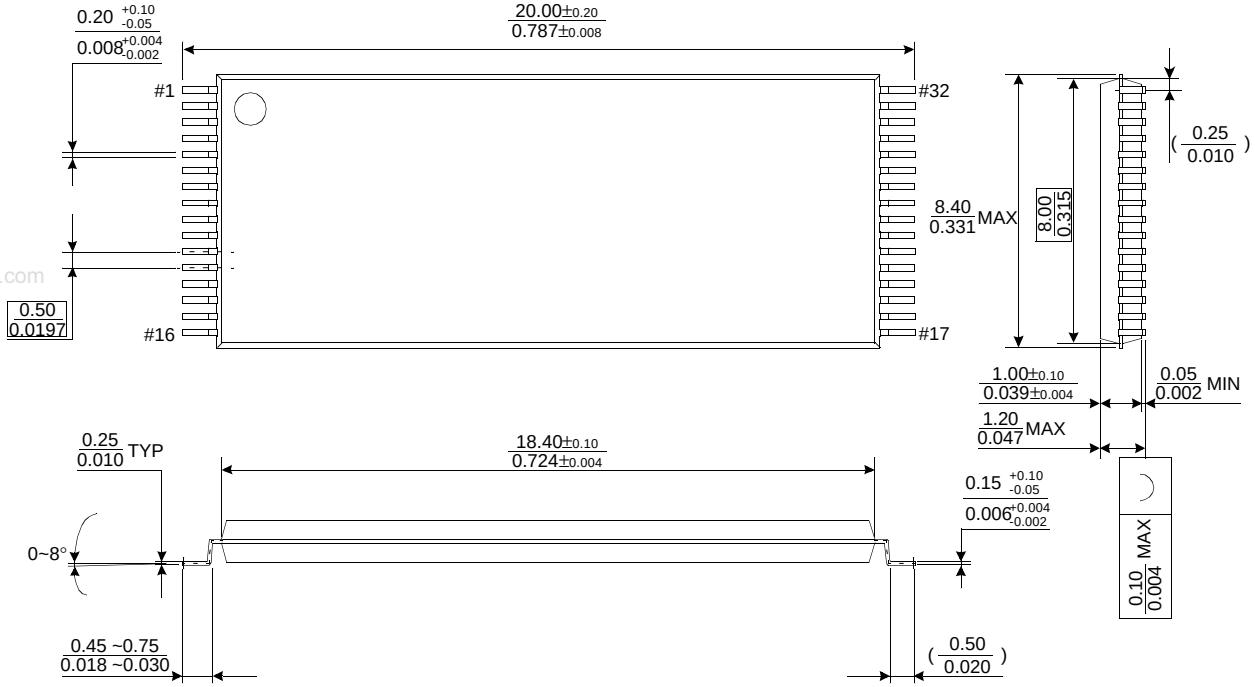
32 PLASTIC SMALL OUTLINE PACKAGE (525mil)



PACKAGE DIMENSIONS

Units: millimeter(inch)

32 THIN SMALL OUTLINE PACKAGE TYPE1 (0820F)



32 THIN SMALL OUTLINE PACKAGE TYPE1 (0820R)