

Document Title

32Kx8 bit Low Power CMOS Static RAM

Revision History

<u>Revision No</u>	<u>History</u>	<u>Draft Data</u>	<u>Remark</u>
0.0	Initial draft	May 18, 1997	Design target
0.1	First revision - KM62256DL/DLI I <sub>SB1</sub> = 100 → 50μA KM62256DL-L I <sub>SB1</sub> = 20 → 10μA KM62256DLI-L I <sub>SB1</sub> = 50 → 15μA - C <sub>IN</sub> = 6 → 8pF, C <sub>IO</sub> = 8 → 10pF - KM62256D-4/5/7 Family t <sub>OH</sub> = 5 → 10ns - KM62256DL/DLI I <sub>DR</sub> = 50 → 30μA KM62256DL-L/DLI-L I <sub>DR</sub> = 30 → 15μA	April 1, 1997	Preliminary
1.0	Finalize - Remove I <sub>CC</sub> write value - Improved operating current I <sub>CC2</sub> = 70 → 60mA - Improved standby current KM62256DL/DLI I <sub>SB1</sub> = 50 → 30μA KM62256DL-L I <sub>SB1</sub> = 10 → 5μA KM62256DLI-L I <sub>SB1</sub> = 15 → 5μA - Improved data retention current KM62256DL/DLI I <sub>DR</sub> = 30 → 5μA KM62256DL-L/DLI-L I <sub>DR</sub> = 15 → 3μA - Remove 45ns part from commercial product and 100ns part from industrial product. Replace test load 100pF to 50pF for 55ns part	November 11, 1997	Final

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## 32Kx8 bit Low Power CMOS Static RAM

### FEATURES

- Process Technology : TFT
- Organization : 32Kx8
- Power Supply Voltage : 4.5~5.5V
- Low Data Retention Voltage : 2V(Min)
- Three state output and TTL Compatible
- Package Type : 28-DIP-600B, 28-SOP-450  
28-TSOP1-0813.4 F/R

### GENERAL DESCRIPTION

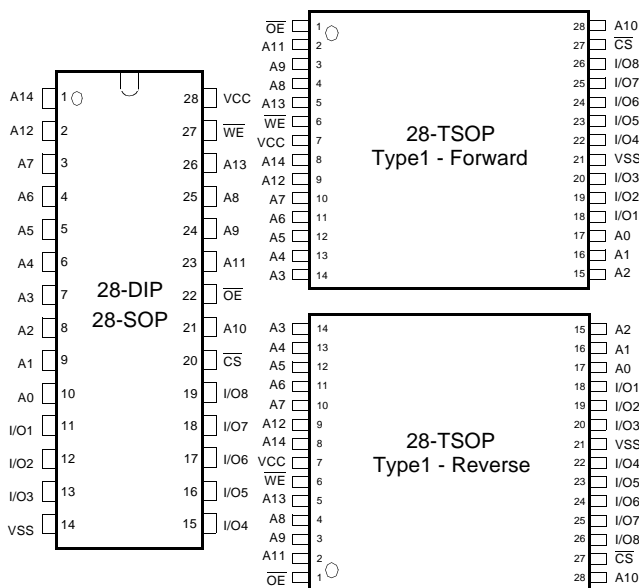
The KM62256D families are fabricated by SAMSUNG's advanced CMOS process technology. The families support various operating temperature ranges and have various package types for user flexibility of system design. The families also support low data retention voltage for battery back-up operation with low data retention current.

### PRODUCT FAMILY

Product Family	Operating Temperature	Vcc Range	Speed	Power Dissipation		PKG Type
				Standby (I <sub>SB1</sub> , Max)	Operating (I <sub>CC2</sub> , Max)	
KM62256DL KM62256DL-L	Commercial (0~70°C)	4.5 to 5.5V	55 <sup>1)</sup> /70ns	30μA 5μA	60mA	28-DIP, 28-SOP 28-TSOP1-F/R
KM62256DLI KM62256DLI-L	Industrial (-40~85°C)		70ns	30μA 5μA		28-SOP 28-TSOP1-F/R

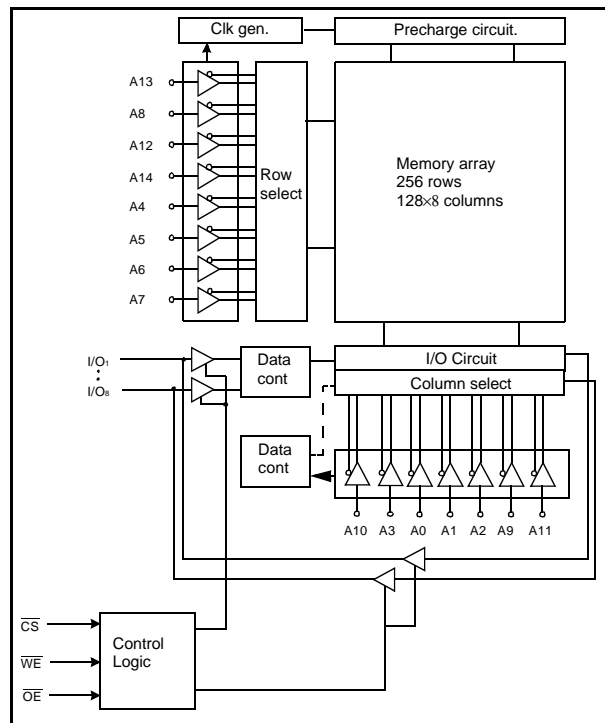
1. The parameter is tested with 50pF test load.

### PIN DESCRIPTION



Pin Name	Function	Pin Name	Function
$\overline{CS}$	Chip Select Input	I/O <sub>1</sub> ~I/O <sub>8</sub>	Data Inputs/Outputs
$\overline{OE}$	Output Enable Input	Vcc	Power
$\overline{WE}$	Write Enable Input	Vss	Ground
A <sub>0</sub> ~A <sub>14</sub>	Address Inputs	NC	No connect

### FUNCTIONAL BLOCK DIAGRAM



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## PRODUCT LIST

Commercial Temperature Products(0~70°C)		Industrial Temperature Products(-40~85°C)	
Part Name	Function	Part Name	Function
KM62256DLP-5	28-DIP, 55ns, L-pwr	KM62256DLGI-7	28-SOP, 70ns, L-pwr
KM62256DLP-5L	28-DIP, 55ns, LL-pwr	KM62256DLGI-7L	28-SOP, 70ns, LL-pwr
KM62256DLP-7	28-DIP, 70ns, L-pwr	KM62256DLTGI-7	28-TSOP1 F, 70ns, L-pwr
KM62256DLP-7L	28-DIP, 70ns, LL-pwr	KM62256DLTGI-7L	28-TSOP1 F, 70ns, LL-pwr
KM62256DLG-5	28-SOP, 50ns, L-pwr	KM62256DLRGI-7	28-TSOP1 R, 70ns, L-pwr
KM62256DLG-5L	28-SOP, 50ns, LL-pwr	KM62256DLRGI-7L	28-TSOP1 R, 70ns, LL-pwr
KM62256DLG-7	28-SOP, 70ns, L-pwr		
KM62256DLG-7L	28-SOP, 70ns, LL-pwr		
KM62256DLTG-5	28-TSOP1 F, 55ns, L-pwr		
KM62256DLTG-5L	28-TSOP1 F, 55ns, LL-pwr		
KM62256DLTG-7	28-TSOP1 F, 70ns, L-pwr		
KM62256DLTG-7L	28-TSOP1 F, 70ns, LL-pwr		
KM62256DLRG-5	28-TSOP1 R, 55ns, L-pwr		
KM62256DLRG-5L	28-TSOP1 R, 55ns, LL-pwr		
KM62256DLRG-7	28-TSOP1 R, 70ns, L-pwr		
KM62256DLRG-7L	28-TSOP1 R, 70ns, LL-pwr		

## FUNCTIONAL DESCRIPTION

$\overline{\text{CS}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	I/O	Mode	Power
H	X <sup>1)</sup>	X <sup>1)</sup>	High-Z	Deselected	Standby
L	H	H	High-Z	Output Disabled	Active
L	L	H	Dout	Read	Active
L	X <sup>1)</sup>	L	Din	Write	Active

1. X means don't care (Must be in high or low states)

## ABSOLUTE MAXIMUM RATINGS<sup>1)</sup>

Item	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to Vss	V <sub>IN</sub> , V <sub>OUT</sub>	-0.5 to 7.0	V	-
Voltage on Vcc supply relative to Vss	V <sub>CC</sub>	-0.5 to 7.0	V	-
Power Dissipation	P <sub>D</sub>	1.0	W	-
Storage temperature	T <sub>STG</sub>	-65 to 150	°C	-
Operating Temperature	T <sub>A</sub>	0 to 70	°C	KM62256DL
		-40 to 85	°C	KM62256DLI
Soldering temperature and time	T <sub>SOLDER</sub>	260°C, 10sec (Lead Only)	-	-

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## RECOMMENDED DC OPERATING CONDITIONS<sup>1)</sup>

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V <sub>cc</sub>	4.5	5.0	5.5	V
Ground	V <sub>ss</sub>	0	0	0	V
Input high voltage	V <sub>IH</sub>	2.2	-	V <sub>cc</sub> +0.5V <sup>2)</sup>	V
Input low voltage	V <sub>IL</sub>	-0.5 <sup>3)</sup>	-	0.8	V

Note:

- Commercial Product : T<sub>A</sub>=0 to 70°C, otherwise specified  
Industrial Product : T<sub>A</sub>=-40 to 85°C, otherwise specified
- Overshoot : V<sub>cc</sub>+3.0V in case of pulse width≤30ns
- Undershoot : -3.0V in case of pulse width≤30ns
- Overshoot and undershoot are sampled, not 100% tested

## CAPACITANCE<sup>1)</sup> (f=1MHz, T<sub>A</sub>=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C <sub>IN</sub>	V <sub>IN</sub> =0V	-	8	pF
Input/Output capacitance	C <sub>IO</sub>	V <sub>IO</sub> =0V	-	10	pF

- Capacitance is sampled not, 100% tested

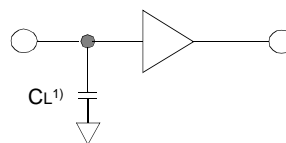
## DC AND OPERATING CHARACTERISTICS

Item	Symbol	Test Conditions	Min	Typ	Max	Unit	
Input leakage current	I <sub>LI</sub>	V <sub>IN</sub> =V <sub>ss</sub> to V <sub>cc</sub>	-1	-	1	μA	
Output leakage current	I <sub>LO</sub>	$\overline{CS}$ =V <sub>IH</sub> or $\overline{OE}$ =V <sub>IH</sub> or $\overline{WE}$ =V <sub>IL</sub> , V <sub>IO</sub> =V <sub>ss</sub> to V <sub>cc</sub>	-1	-	1	μA	
Operating power supply current	I <sub>CC</sub>	I <sub>IO</sub> =0mA, $\overline{CS}$ =V <sub>IL</sub> , V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> , Read	-	5	10	mA	
Average operating current	I <sub>CC1</sub>	Cycle time=1μs, 100% duty, I <sub>IO</sub> =0mA $\overline{CS}$ ≤0.2V, V <sub>IN</sub> ≤0.2V, V <sub>IN</sub> ≥V <sub>cc</sub> -0.2V	Read	-	2	5	mA
			Write	-	-	20	
	I <sub>CC2</sub>	Cycle time=Min, 100% duty, I <sub>IO</sub> =0mA, $\overline{CS}$ =V <sub>IL</sub> , V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub>	-	45	60	mA	
Output low voltage	V <sub>OL</sub>	I <sub>OL</sub> =2.1mA	-	-	0.4	V	
Output high voltage	V <sub>OH</sub>	I <sub>OH</sub> =-1.0mA	2.4	-	-	V	
Standby Current(TTL)	I <sub>SB</sub>	$\overline{CS}$ =V <sub>IH</sub> , Other inputs=V <sub>IH</sub> or V <sub>IL</sub>	-	-	1	mA	
Standby Current (CMOS)	I <sub>SB1</sub>	$\overline{CS}$ ≥V <sub>cc</sub> -0.2V, Other inputs=0~V <sub>cc</sub>	Low Power	-	1	30	μA
			Low Low Power	-	0.2	5	μA

## AC OPERATING CONDITIONS

### TEST CONDITIONS (Test Load and Test Input/Output Reference)

Input pulse level : 0.8 to 2.4V  
 Input rising and falling time : 5ns  
 Input and output reference voltage : 1.5V  
 Output load (See right) :  $C_L=100\text{pF}+1\text{TTL}$   
 $C_L=50\text{pF}+1\text{TTL}$



1. Including scope and jig capacitance

## AC CHARACTERISTICS ( $V_{CC}=4.5\sim 5.5\text{V}$ , KM62256D Family: $T_A=0$ to $70^\circ\text{C}$ , KM62256DI Family: $T_A=-40$ to $85^\circ\text{C}$ )

Parameter List		Symbol	Speed Bins				Units
			55 <sup>1)</sup> ns		70ns		
			Min	Max	Min	Max	
Read	Read cycle time	t <sub>RC</sub>	55	-	70	-	ns
	Address access time	t <sub>AA</sub>	-	55	-	70	ns
	Chip select to output	t <sub>CO</sub>	-	55	-	70	ns
	Output enable to valid output	t <sub>OE</sub>	-	25	-	35	ns
	Chip select to low-Z output	t <sub>LZ</sub>	10	-	10	-	ns
	Output enable to low-Z output	t <sub>OLZ</sub>	5	-	5	-	ns
	Chip disable to high-Z output	t <sub>HZ</sub>	0	20	0	30	ns
	Output disable to high-Z output	t <sub>OHZ</sub>	0	20	0	30	ns
Write	Output hold from address change	t <sub>OH</sub>	10	-	10	-	ns
	Write cycle time	t <sub>WC</sub>	55	-	70	-	ns
	Chip select to end of write	t <sub>CW</sub>	45	-	60	-	ns
	Address set-up time	t <sub>AS</sub>	0	-	0	-	ns
	Address valid to end of write	t <sub>AW</sub>	45	-	60	-	ns
	Write pulse width	t <sub>WP</sub>	40	-	50	-	ns
	Write recovery time	t <sub>WR</sub>	0	-	0	-	ns
	Write to output high-Z	t <sub>WHZ</sub>	0	20	0	25	ns
	Data to write time overlap	t <sub>DW</sub>	25	-	30	-	ns
	Data hold from write time	t <sub>DH</sub>	0	-	0	-	ns
End write to output low-Z	t <sub>OW</sub>	5	-	5	-	ns	

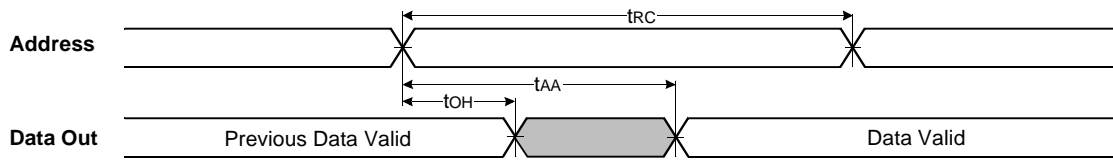
1. The parameter is tested with 50pF test load.

## DATA RETENTION CHARACTERISTICS

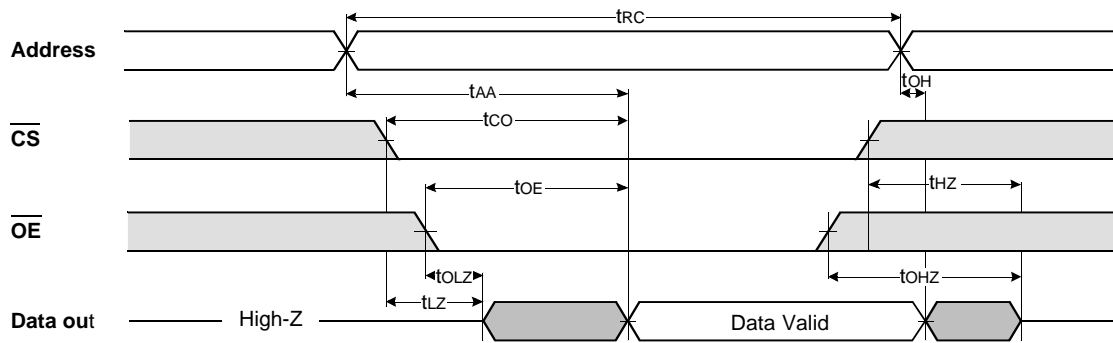
Item	Symbol	Test Condition	Min	Typ	Max	Unit	
V <sub>CC</sub> for data retention	V <sub>DR</sub>	$\overline{CS} \geq V_{CC}-0.2\text{V}$	2.0	-	5.5	V	
Data retention current	I <sub>DR</sub>	$V_{CC}=3.0\text{V}, \overline{CS} \geq V_{CC}-0.2\text{V}$	L-Ver	-	1	15	$\mu\text{A}$
			LL-Ver	-	0.2	3	
Data retention set-up time	t <sub>SDR</sub>	See data retention waveform	0	-	-	ms	
Recovery time	t <sub>RDR</sub>		5	-	-		

TIMMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled,  $\overline{CS}=\overline{OE}=V_{IL}$ ,  $\overline{WE}=V_{IH}$ )



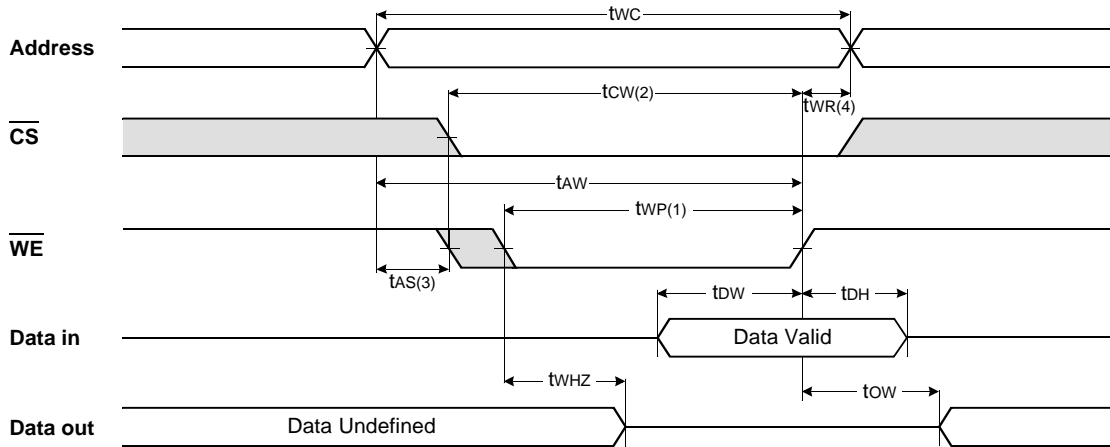
TIMING WAVEFORM OF READ CYCLE(2) ( $\overline{WE}=V_{IH}$ )



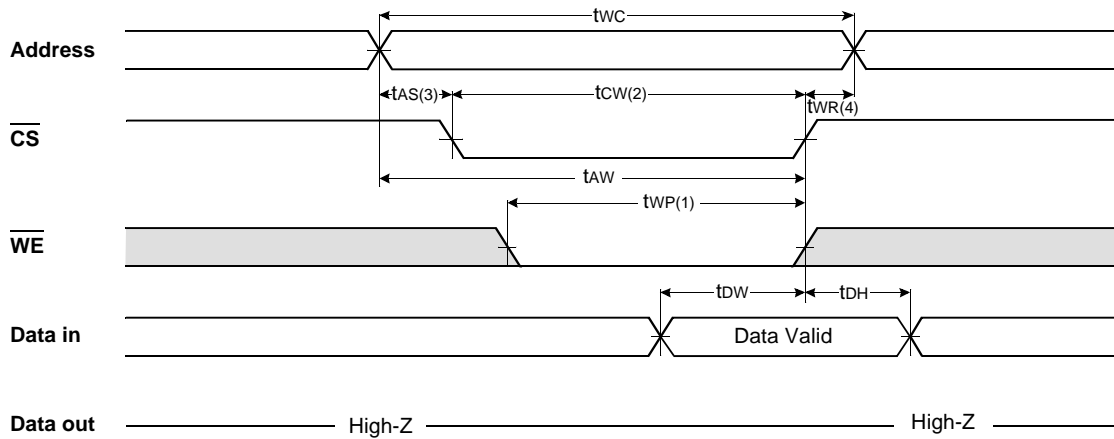
NOTES (READ CYCLE)

1.  $t_{HZ}$  and  $t_{OZH}$  are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition,  $t_{HZ}(\text{Max.})$  is less than  $t_{LZ}(\text{Min.})$  both for a given device and from device to device interconnection.

## TIMING WAVEFORM OF WRITE CYCLE(1) (WE Controlled)



## TIMING WAVEFORM OF WRITE CYCLE(2) ( $\overline{CS}$ Controlled)

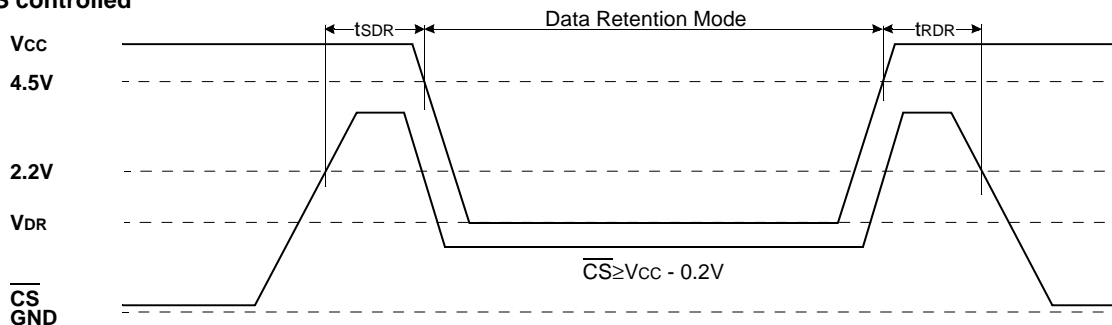


### NOTES (WRITE CYCLE)

1. A write occurs during the overlap of a low  $\overline{CS}$  and a low  $\overline{WE}$ . A write begins at the latest transition among  $\overline{CS}$  going Low and  $\overline{WE}$  going low : A write ends at the earliest transition among CS going high and WE going high,  $t_{WP}$  is measured from the beginning of write to the end of write.
2.  $t_{OW}$  is measured from the  $\overline{CS}$  going low to end of write.
3.  $t_{AS}$  is measured from the address valid to the beginning of write.
4.  $t_{WR}$  is measured from the end of write to the address change.  $t_{WR}$  applied in case a write ends as  $\overline{CS}$  or  $\overline{WE}$  going high.

## DATA RETENTION WAVE FORM

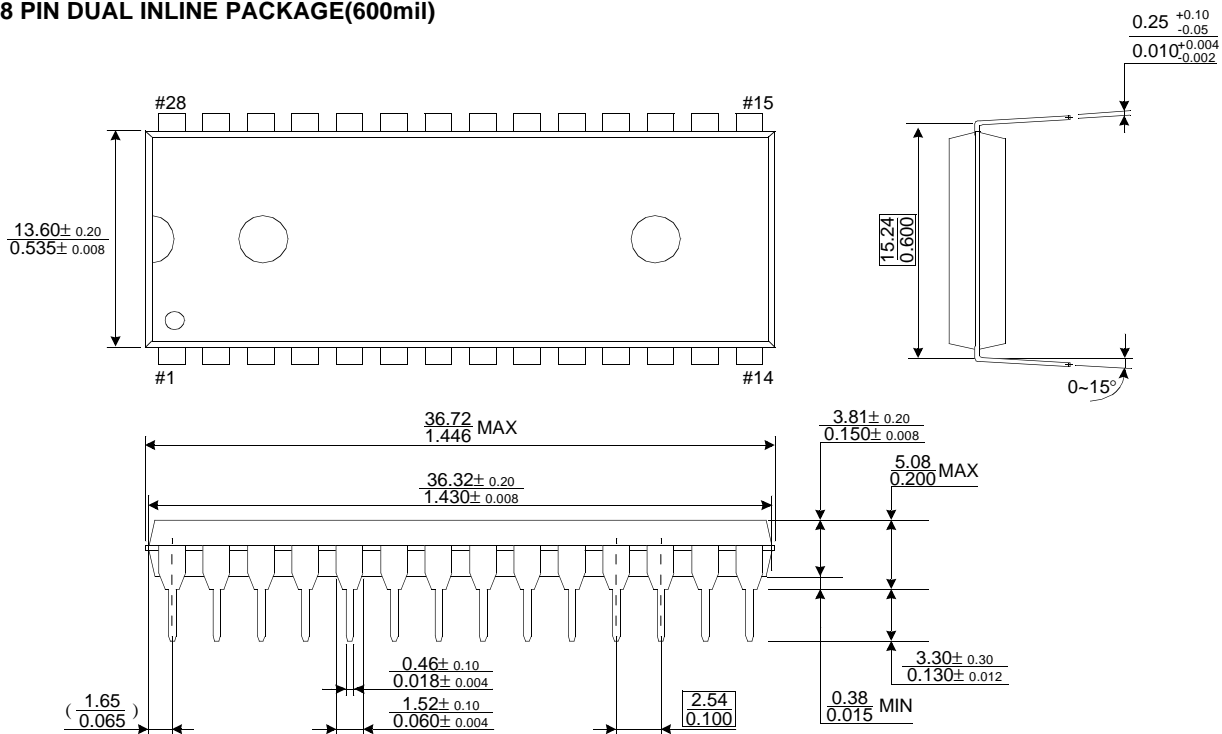
### $\overline{CS}$ controlled



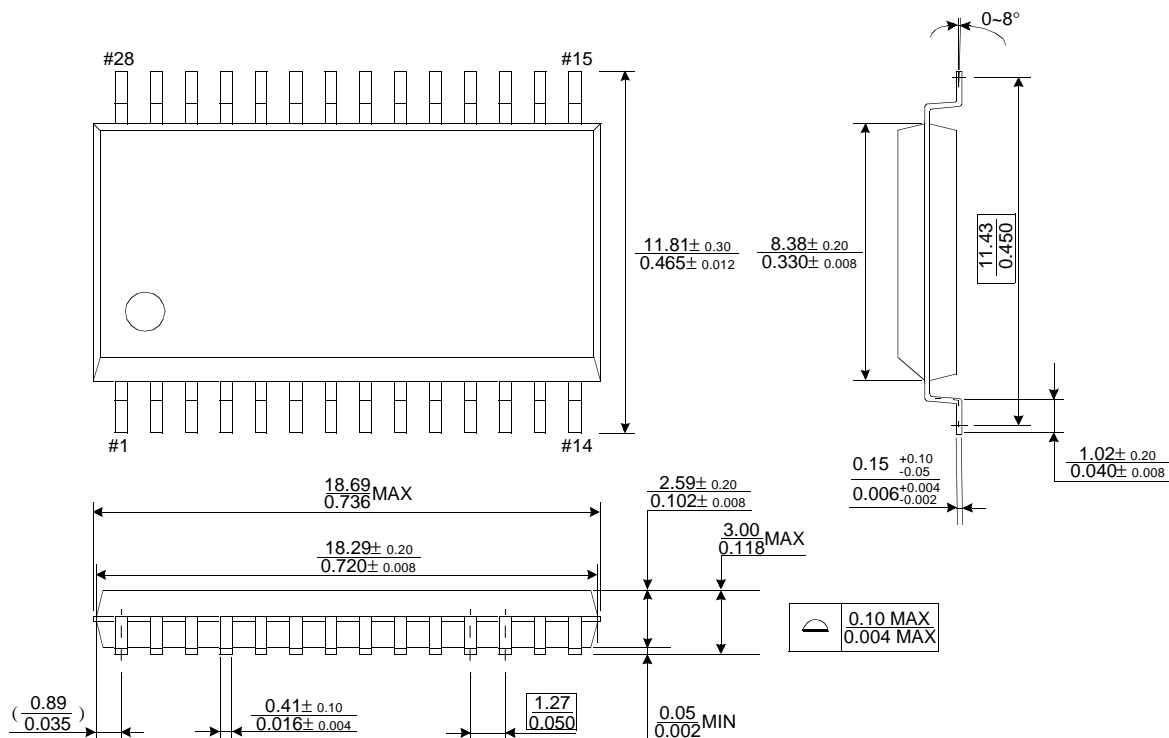
## PACKAGE DIMENSIONS

Units: millimeter(inch)

### 28 PIN DUAL INLINE PACKAGE(600mil)



### 28 PIN PLASTIC SMALL OUTLINE PACKAGE(450mil)





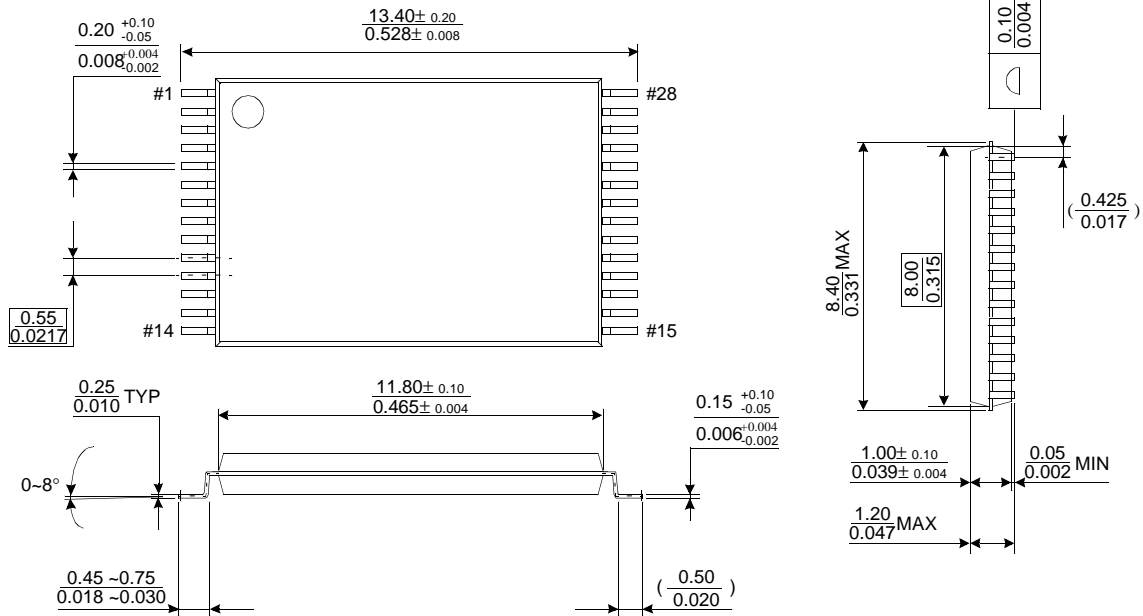
# KM62256D Family

# CMOS SRAM

## PACKAGE DIMENSIONS

Units: millimeter(inch)

### 28 PIN THIN SMALL OUTLINE PACKAGE TYPE1 (0813.4F)



### 28 PIN THIN SMALL OUTLINE PACKAGE TYPE1 (0813.4R)

