## Document Title

**1Mx4 Bit High Speed Static RAM(5.0V Operating).**
**Operated at Commercial and Industrial Temperature Ranges.**

## Revision History

| RevNo. | History | Draft Data | Remark |
|---|---|---|---|
| Rev. 0.0 | Initial release with Preliminary. | September. 7. 2001 | Preliminary |
| Rev. 0.1 | Change Icc. Isb and Isb1 | November, 3. 2001 | Preliminary |

| Item | | Previous | Current |
|---|---|---|---|
| $I_{CC}$(Commercial) | 10ns | 90mA | 65mA |
| | 12ns | 80mA | 55mA |
| | 15ns | 70mA | 45mA |
| $I_{CC}$(Industrial) | 10ns | 115mA | 85mA |
| | 12ns | 100mA | 75mA |
| | 15ns | 85mA | 65mA |
| $I_{SB}$ | | 30mA | 20mA |
| $I_{SB1}$ | | 10mA | 5mA |

| | | | |
|---|---|---|---|
| Rev. 0.2 | 1. Correct AC parameters : Read & Write Cycle mA<br>2. Delete Low Ver.<br>3. Delete Data Retention Characteristics | November, 3. 2001 | Preliminary |
| Rev. 0.3 | 1. Delete 15ns speed bin.<br>2. Change Icc for Industrial mode. | December, 18. 2001 | Preliminary |

| Item | | Previous | Current |
|---|---|---|---|
| $I_{CC}$(Industrial) | 10ns | 85mA | 75mA |
| | 12ns | 75mA | 65mA |

| | | | |
|---|---|---|---|
| Rev. 1.0 | 1. Final datasheet release.<br>2. Delete 12ns speed bin.<br>3. Delete UB,LB releated AC characteristics and timing diagram.<br>4. Correct Read Cycle time waveform(2). | July, 09, 2002 | Final |

## 4Mb Async. Fast SRAM Ordering Information

| Org. | Part Number | VDD(V) | Speed ( ns ) | PKG | Temp. & Power |
|---|---|---|---|---|---|
| 1M x4 | K6R4004C1D-JC(I) 10 | 5 | 10 | J : 32-SOJ | C : Commercial Temperature ,Normal Power Range<br>I : Industrial Temperature ,Normal Power Range<br>L : Commercial Temperature ,Low Power Range<br>P : Industrial Temperature ,Low Power Range |
| | K6R4004V1D-JC(I) 08/10 | 3.3 | 8/10 | | |
| 512K x8 | K6R4008C1D-J(T)C(I) 10 | 5 | 10 | J : 36-SOJ<br>T : 44-TSOP2 | |
| | K6R4008V1D-J(T)C(I) 08/10 | 3.3 | 8/10 | | |
| 256K x16 | K6R4016C1D-J(T,E)C(I) 10 | 5 | 10 | J : 44-SOJ<br>T : 44-TSOP2<br>E : 48-TBGA | |
| | K6R4016V1D-J(T,E)C(I,L,P) 08/10 | 3.3 | 8/10 | | |

## *1M x 4 Bit High-Speed CMOS Static RAM*

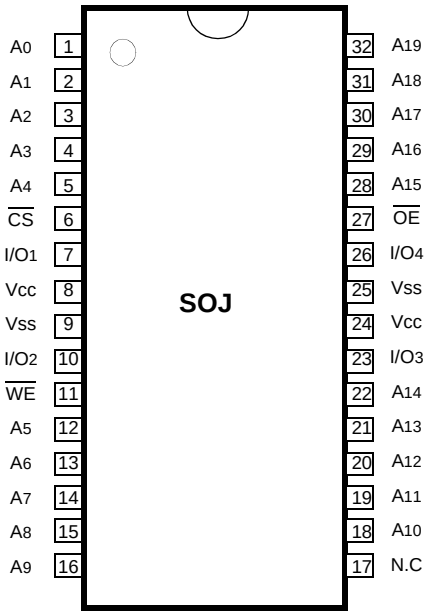
### FEATURES

- Fast Access Time 10ns(Max.)
- Low Power Dissipation
  Standby (TTL) : 20mA(Max.)
  (CMOS) : 5mA(Max.)
  Operating K6R4004C1D-10 : 65mA(Max.)
  Single 5.0V±10% Power Supply
- TTL Compatible Inputs and Outputs
- Fully Static Operation
  - No Clock or Refresh required
- Three State Outputs
- Center Power/Ground Pin Configuration
- Standard Pin Configuration
  K6R4004C1D-J : 32-SOJ-400
- Operating in Commercial and Industrial Temperature range.

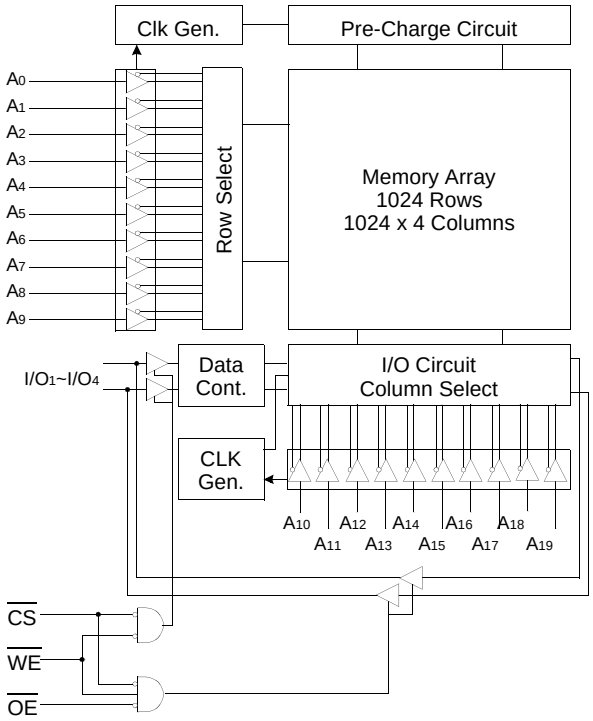
### GENERAL DESCRIPTION

The K6R4004C1D is a 4,194,304-bit high-speed Static Random Access Memory organized as 1,048,576 words by 4 bits. The K6R4004C1D uses 4 common input and output lines and has an output enable pin which operates faster than address access time at read cycle. The device is fabricated using SAMSUNG′s advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The K6R4004C1D is packaged in a 400 mil 32-pin plastic SOJ.

### PIN CONFIGURATION *(Top View)*




### FUNCTIONAL BLOCK DIAGRAM




### PIN FUNCTION

| Pin Name | Pin Function |
|---|---|
| A0 - A19 | Address Inputs |
| $\overline{WE}$ | Write Enable |
| $\overline{CS}$ | Chip Select |
| $\overline{OE}$ | Output Enable |
| I/O1 ~ I/O4 | Data Inputs/Outputs |
| Vcc | Power(+5.0V) |
| Vss | Ground |
| N.C | No Connection |



SAMSUNG ELECTRONICS

## ABSOLUTE MAXIMUM RATINGS*

| Parameter | | Symbol | Rating | Unit |
|---|---|---|---|---|
| Voltage on Any Pin Relative to $V_{SS}$ | | $V_{IN}$, $V_{OUT}$ | -0.5 to $V_{CC}$+0.5 | V |
| Voltage on $V_{CC}$ Supply Relative to $V_{SS}$ | | $V_{CC}$ | -0.5 to 7.0 | V |
| Power Dissipation | | $P_D$ | 1.0 | W |
| Storage Temperature | | $T_{STG}$ | -65 to 150 | °C |
| Operating Temperature | Commercial | $T_A$ | 0 to 70 | °C |
| | Industrial | $T_A$ | -40 to 85 | °C |

***** Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## RECOMMENDED DC OPERATING CONDITIONS*($T_A$=0 to 70°C)

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | 4.5 | 5.0 | 5.5 | V |
| Ground | $V_{SS}$ | 0 | 0 | 0 | V |
| Input High Voltage | $V_{IH}$ | 2.2 | - | $V_{CC}$+0.5** | V |
| Input Low Voltage | $V_{IL}$ | -0.5* | - | 0.8 | V |

* The above parameters are also guaranteed at industrial temperature range.
****** $V_{IL}$(Min) = -2.0V a.c(Pulse Width ≤ 8ns) for I ≤ 20mA.
******* $V_{IH}$(Max) = $V_{CC}$ + 2.0V a.c (Pulse Width ≤ 8ns) for I ≤ 20mA.

## DC AND OPERATING CHARACTERISTICS*($T_A$=0 to 70°C, Vcc=5.0V±10%, unless otherwise specified)

| Parameter | Symbol | Test Conditions | | | Min | Max | Unit |
|---|---|---|---|---|---|---|---|
| Input Leakage Current | $I_{LI}$ | $V_{IN}$=$V_{SS}$ to $V_{CC}$ | | | -2 | 2 | µA |
| Output Leakage Current | $I_{LO}$ | $\overline{CS}$=$V_{IH}$ or $\overline{OE}$=$V_{IH}$ or $\overline{WE}$=$V_{IL}$<br>$V_{OUT}$=$V_{SS}$ to $V_{CC}$ | | | -2 | 2 | µA |
| Operating Current | $I_{CC}$ | Min. Cycle, 100% Duty<br>$\overline{CS}$=$V_{IL}$, $V_{IN}$=$V_{IH}$ or $V_{IL}$, $I_{OUT}$=0mA | Com. | 10ns | - | 65 | mA |
| | | | Ind. | 10ns | - | 75 | |
| Standby Current | $I_{SB}$ | Min. Cycle, $\overline{CS}$=$V_{IH}$ | | | - | 20 | mA |
| | $I_{SB1}$ | f=0MHz, $\overline{CS}$≥$V_{CC}$-0.2V,<br>$V_{IN}$≥$V_{CC}$-0.2V or $V_{IN}$≤0.2V | | | - | 5 | |
| Output Low Voltage Level | $V_{OL}$ | $I_{OL}$=8mA | | | - | 0.4 | V |
| Output High Voltage Level | $V_{OH}$ | $I_{OH}$=-4mA | | | 2.4 | - | V |

* The above parameters are also guaranteed at industrial temperature range.

## CAPACITANCE*($T_A$=25°C, f=1.0MHz)

| Item | Symbol | Test Conditions | MIN | Max | Unit |
|---|---|---|---|---|---|
| Input/Output Capacitance | $C_{I/O}$ | $V_{I/O}$=0V | - | 8 | pF |
| Input Capacitance | $C_{IN}$ | $V_{IN}$=0V | - | 6 | pF |

* Capacitance is sampled and not 100% tested.

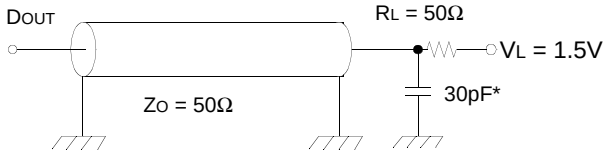
## AC CHARACTERISTICS($T_A$=0 to 70°C, $V_{CC}$=5.0V±10%, unless otherwise noted.)

### TEST CONDITIONS*

| Parameter | Value |
|---|---|
| Input Pulse Levels | 0V to 3V |
| Input Rise and Fall Times | 3ns |
| Input and Output timing Reference Levels | 1.5V |
| Output Loads | See below |

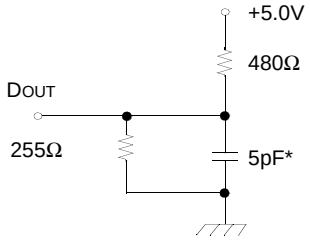
* The above test conditions are also applied at industrial temperature range.

Output Loads(A)




* Capacitive Load consists of all components of the test environment.

Output Loads(B)
for $t_{HZ}$, $t_{LZ}$, $t_{WHZ}$, $t_{OW}$, $t_{OLZ}$ & $t_{OHZ}$




* Including Scope and Jig Capacitance

### READ CYCLE*

| Parameter | Symbol | K6R4004C1D-10 | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| Read Cycle Time | $t_{RC}$ | 10 | - | ns |
| Address Access Time | $t_{AA}$ | - | 10 | ns |
| Chip Select to Output | $t_{CO}$ | - | 10 | ns |
| Output Enable to Valid Output | $t_{OE}$ | - | 5 | ns |
| Chip Enable to Low-Z Output | $t_{LZ}$ | 3 | - | ns |
| Output Enable to Low-Z Output | $t_{OLZ}$ | 0 | - | ns |
| Chip Disable to High-Z Output | $t_{HZ}$ | 0 | 5 | ns |
| Output Disable to High-Z Output | $t_{OHZ}$ | 0 | 5 | ns |
| Output Hold from Address Change | $t_{OH}$ | 3 | - | ns |
| Chip Selection to Power Up Time | $t_{PU}$ | 0 | - | ns |
| Chip Selection to Power DownTime | $t_{PD}$ | - | 10 | ns |

* The above parameters are also guaranteed at industrial temperature range.

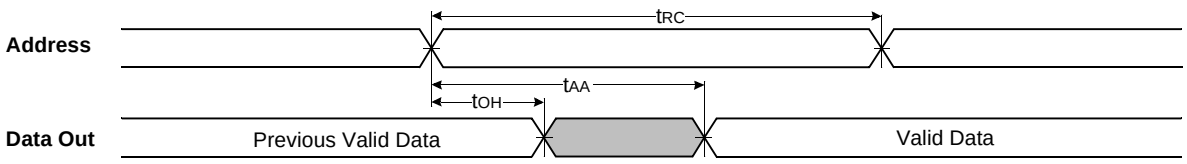
### WRITE CYCLE*

| Parameter | Symbol | K6R4004C1D-10 | | K6R4004C1D-12 | | Unit |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| Write Cycle Time | $t_{WC}$ | 10 | - | 12 | - | ns |
| Chip Select to End of Write | $t_{CW}$ | 7 | - | 8 | - | ns |
| Address Set-up Time | $t_{AS}$ | 0 | - | 0 | - | ns |
| Address Valid to End of Write | $t_{AW}$ | 7 | - | 8 | - | ns |
| Write Pulse Width($\overline{OE}$ High) | $t_{WP}$ | 7 | - | 8 | - | ns |
| Write Pulse Width($\overline{OE}$ Low) | $t_{WP1}$ | 10 | - | 12 | - | ns |
| Write Recovery Time | $t_{WR}$ | 0 | - | 0 | - | ns |
| Write to Output High-Z | $t_{WHZ}$ | 0 | 5 | 0 | 6 | ns |
| Data to Write Time Overlap | $t_{DW}$ | 5 | - | 6 | - | ns |
| Data Hold from Write Time | $t_{DH}$ | 0 | - | 0 | - | ns |
| End of Write to Output Low-Z | $t_{OW}$ | 3 | - | 3 | - | ns |

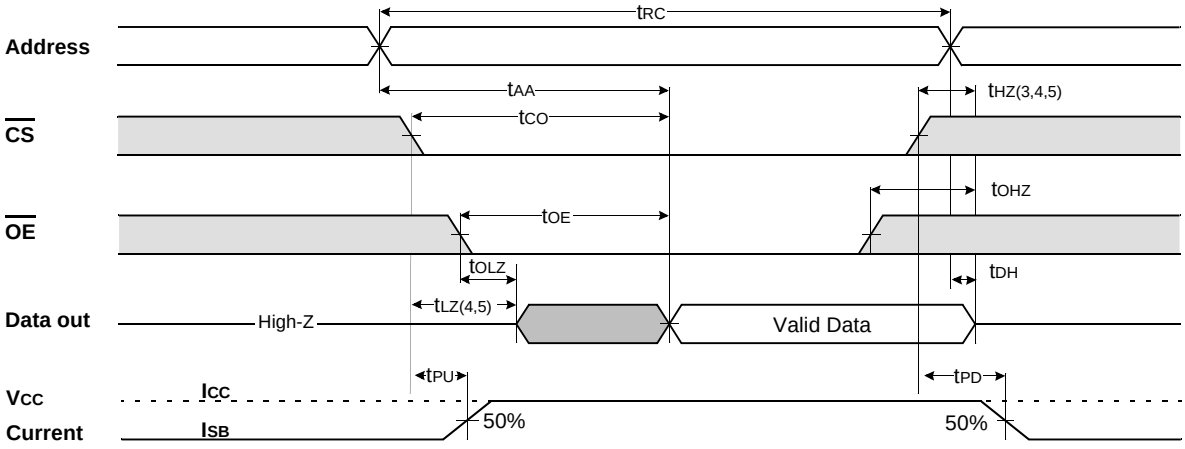
* The above parameters are also guaranteed at industrial temperature range.

## TIMING DIAGRAMS

### TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled, $\overline{CS}$=$\overline{OE}$=$V_{IL}$, $\overline{WE}$=$V_{IH}$)



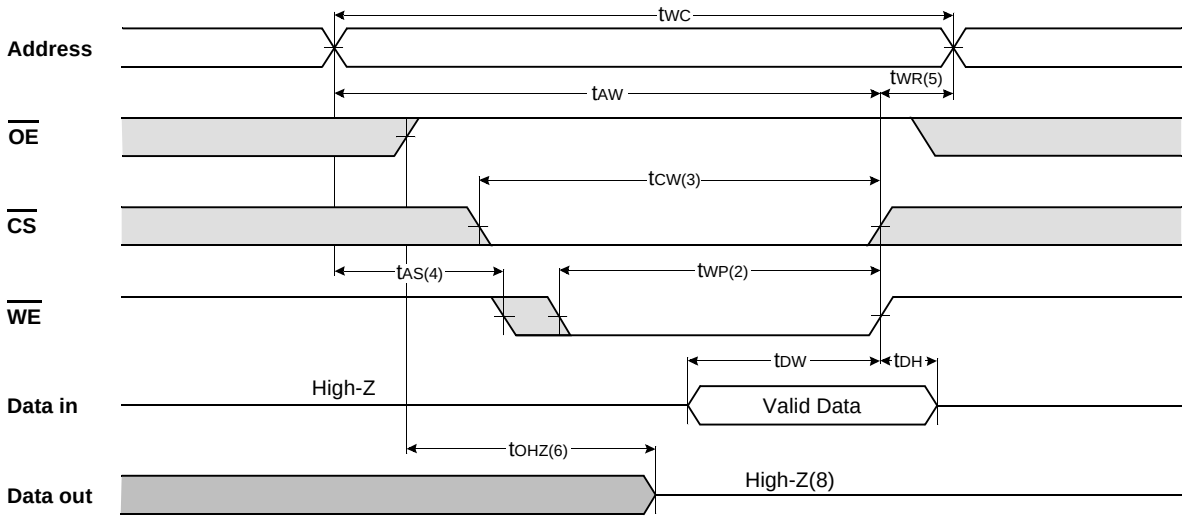

### TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}$=$V_{IH}$)



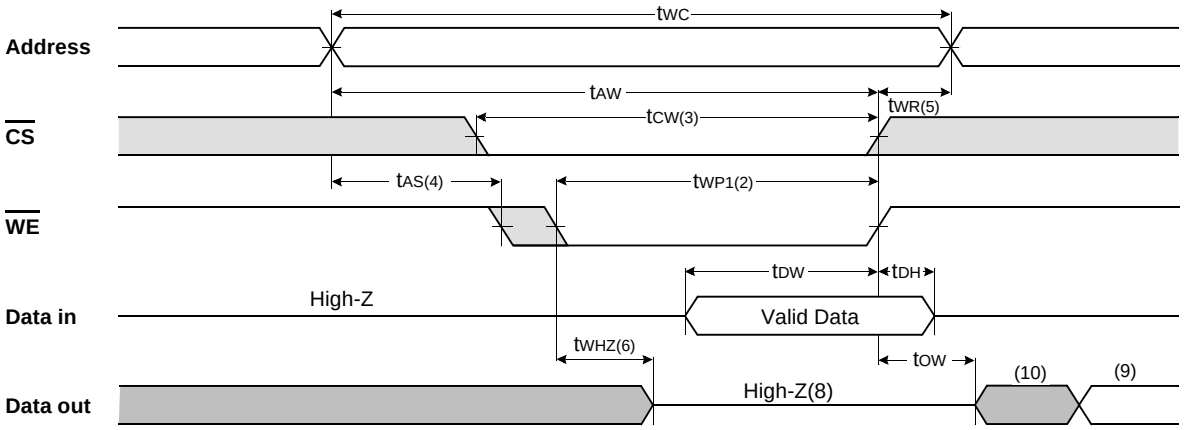

**NOTES**(READ CYCLE)

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. $t_{HZ}$ and $t_{OHZ}$ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to $V_{OH}$ or $V_{OL}$ levels.
4. At any given temperature and voltage condition, $t_{HZ}$(Max.) is less than $t_{LZ}$(Min.) both for a given device and from device to device.
5. Transition is measured ±200mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS}$=$V_{IL}$.
7. Address valid prior to coincident with $\overline{CS}$ transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

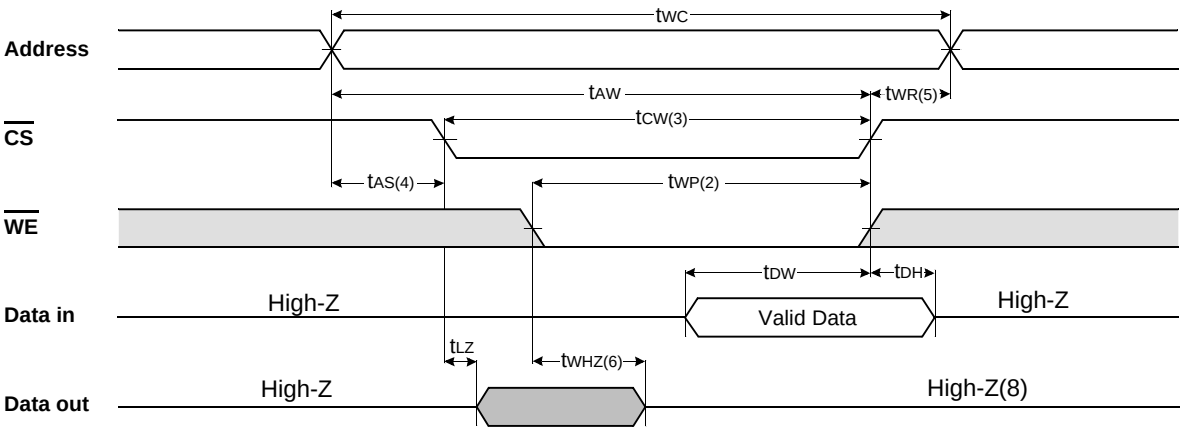
### TIMING WAVEFORM OF WRITE CYCLE(1) ($\overline{OE}$= Clock)




### TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{OE}$=Low Fixed)




### TIMING WAVEFORM OF WRITE CYCLE(3) ($\overline{CS}$=Controlled)



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**NOTES**(WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low $\overline{CS}$ and $\overline{WE}$. A write begins at the latest transition $\overline{CS}$ going low and $\overline{WE}$ going low ; A write ends at the earliest transition $\overline{CS}$ going high or $\overline{WE}$ going high. $t_{WP}$ is measured from the beginning of write to the end of write.
3. $t_{CW}$ is measured from the later of $\overline{CS}$ going low to end of write.
4. $t_{AS}$ is measured from the address valid to the beginning of write.
5. $t_{WR}$ is measured from the end of write to the address change. $t_{WR}$ applied in case a write ends as $\overline{CS}$ or $\overline{WE}$ going high.
6. If $\overline{OE}$, $\overline{CS}$ and $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going or after $\overline{WE}$ going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When $\overline{CS}$ is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

## FUNCTIONAL DESCRIPTION

| $\overline{CS}$ | $\overline{WE}$ | $\overline{OE}$ | Mode | I/O Pin | Supply Current |
|---|---|---|---|---|---|
| H | X | X* | Not Select | High-Z | $I_{SB}$, $I_{SB1}$ |
| L | H | H | Output Disable | High-Z | $I_{CC}$ |
| L | H | L | Read | $D_{OUT}$ | $I_{CC}$ |
| L | L | X | Write | $D_{IN}$ | $I_{CC}$ |

* X means Don't Care.

## PACKAGE DIMENSIONS

Units:millimeters/Inches

### 32-SOJ-400