

## 512K x 8 HIGH-SPEED ASYNCHRONOUS CMOS STATIC RAM

NOVEMBER 2007

### FEATURES

#### HIGH SPEED: (IS61/64WV5128ALL/BLL)

- High-speed access time: 8, 10, 20 ns
- Low Active Power: 85 mW (typical)
- Low stand-by power: 7 mW (typical) CMOS standby

#### LOW POWER: (IS61/64WV5128ALS/BLS)

- High-speed access time: 25, 35 ns
- Low Active Power: 35 mW (typical)
- Low stand-by power: 0.6 mW (typical) CMOS standby
- Single power supply
  - V<sub>DD</sub> 1.65V to 2.2V (IS61WV5128Axx)
  - V<sub>DD</sub> 2.4V to 3.6V (IS61/64WV5128Bxx)
- Fully static operation: no clock or refresh required
- Three state outputs
- Industrial and Automotive temperature support
- Lead-free available

### DESCRIPTION

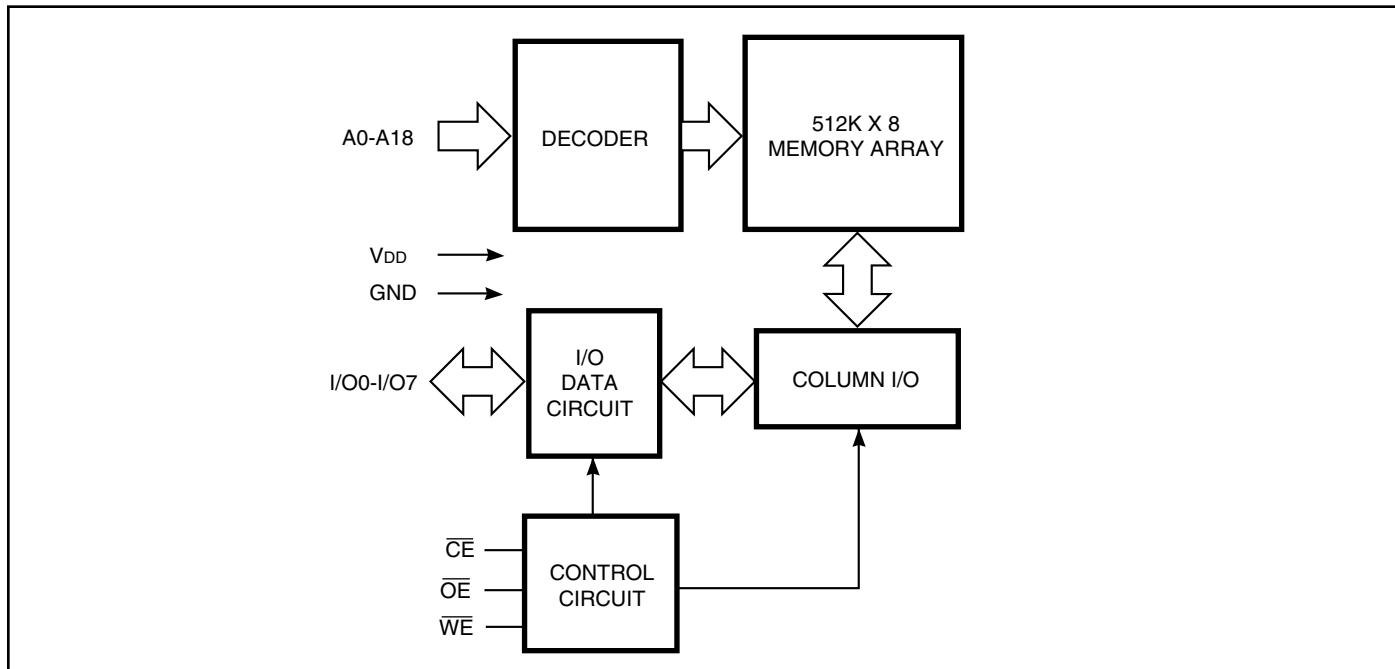
The *ISSI* IS61WV5128Axx and IS61/64WV5128Bxx are very high-speed, low power, 524,288-word by 8-bit CMOS static RAMs. The IS61WV5128Axx and IS61/64WV5128Bxx are fabricated using *ISSI*'s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields higher performance and low power consumption devices.

When  $\overline{CE}$  is HIGH (deselected), the device assumes a standby mode at which the power dissipation can be reduced down with CMOS input levels.

The IS61WV5128Axx and IS61/64WV5128Bxx operate from a single power supply and all inputs are TTL-compatible.

The IS61WV5128Axx and IS61/64WV5128Bxx are available in 36-pin 400-mil SOJ, 36-pin mini BGA, and 44-pin

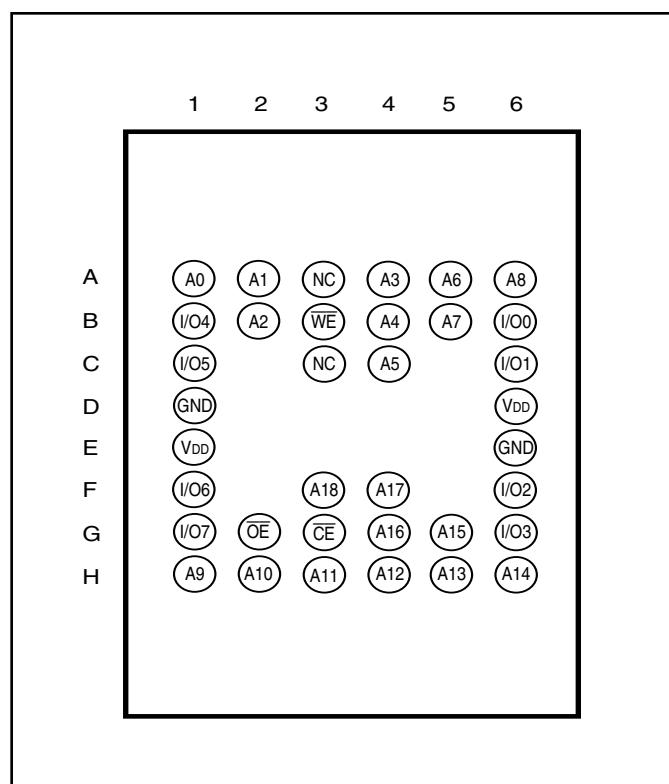
### FUNCTIONAL BLOCK DIAGRAM



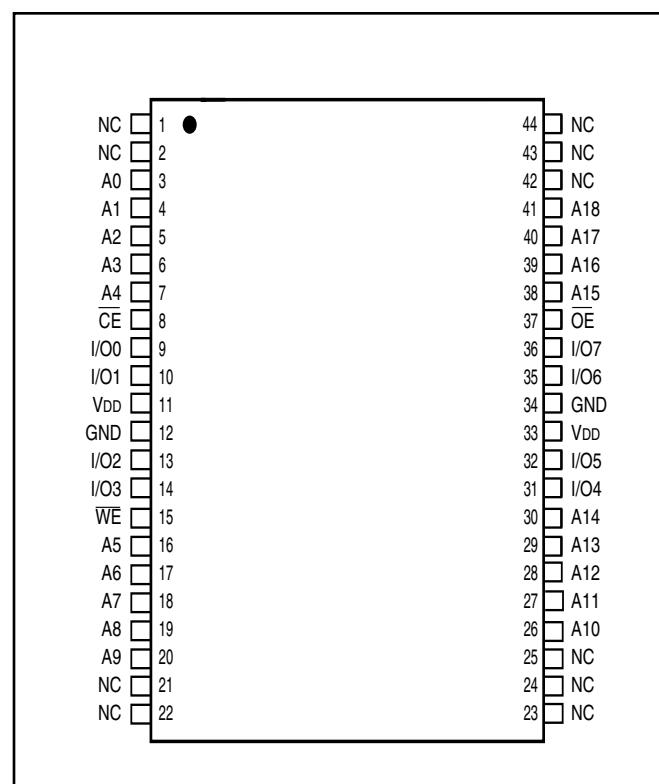
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## PIN CONFIGURATION

36 mini BGA



**44-Pin TSOP (Type II)**



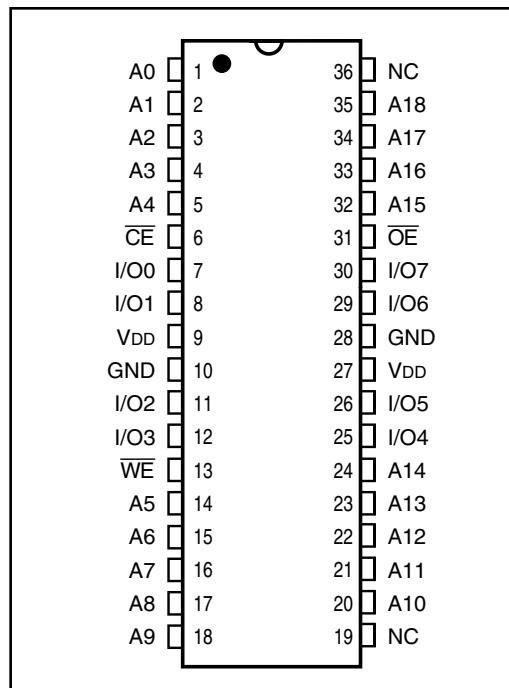
## PIN DESCRIPTIONS

A0-A18	Address Inputs
CE	Chip Enable Input
OE	Output Enable Input
WE	Write Enable Input
I/O0-I/O7	Bidirectional Ports
VDD	Power
GND	Ground
NC	No Connection

## TRUTH TABLE

Mode	WE	CE	OE	I/O Operation	VDD Current
Not Selected (Power-down)	X	H	X	High-Z	I <sub>SB1</sub> , I <sub>SB2</sub>
Output Disabled	H	L	H	High-Z	I <sub>CC</sub>
Read	H	L	L	D <sub>OUT</sub>	I <sub>CC</sub>
Write	L	L	X	D <sub>IN</sub>	I <sub>CC</sub>

**36-Pin SOJ**



**DC ELECTRICAL CHARACTERISTICS** (Over Operating Range)

**V<sub>DD</sub> = 3.3V ± 5%**

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V <sub>OH</sub>	Output HIGH Voltage	V <sub>DD</sub> = Min., I <sub>OH</sub> = -4.0 mA	2.4	—	V
V <sub>OL</sub>	Output LOW Voltage	V <sub>DD</sub> = Min., I <sub>OL</sub> = 8.0 mA	—	0.4	V
V <sub>IH</sub>	Input HIGH Voltage		2	V <sub>DD</sub> + 0.3	V
V <sub>IL</sub>	Input LOW Voltage <sup>(1)</sup>		-0.3	0.8	V
I <sub>LI</sub>	Input Leakage	GND ≤ V <sub>IN</sub> ≤ V <sub>DD</sub>	-1	1	µA
I <sub>LO</sub>	Output Leakage	GND ≤ V <sub>OUT</sub> ≤ V <sub>DD</sub> , Outputs Disabled	-1	1	µA

**Note:**

1. V<sub>IL</sub> (min.) = -0.3V DC; V<sub>IL</sub> (min.) = -2.0V AC (pulse width <10 ns). Not 100% tested.  
 V<sub>IH</sub> (max.) = V<sub>DD</sub> + 0.3V DC; V<sub>IH</sub> (max.) = V<sub>DD</sub> + 2.0V AC (pulse width <10 ns). Not 100% tested.

**DC ELECTRICAL CHARACTERISTICS** (Over Operating Range)

**V<sub>DD</sub> = 2.4V-3.6V**

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V <sub>OH</sub>	Output HIGH Voltage	V <sub>DD</sub> = Min., I <sub>OH</sub> = -1.0 mA	1.8	—	V
V <sub>OL</sub>	Output LOW Voltage	V <sub>DD</sub> = Min., I <sub>OL</sub> = 1.0 mA	—	0.4	V
V <sub>IH</sub>	Input HIGH Voltage		2.0	V <sub>DD</sub> + 0.3	V
V <sub>IL</sub>	Input LOW Voltage <sup>(1)</sup>		-0.3	0.8	V
I <sub>LI</sub>	Input Leakage	GND ≤ V <sub>IN</sub> ≤ V <sub>DD</sub>	-1	1	µA
I <sub>LO</sub>	Output Leakage	GND ≤ V <sub>OUT</sub> ≤ V <sub>DD</sub> , Outputs Disabled	-1	1	µA

**Note:**

1. V<sub>IL</sub> (min.) = -0.3V DC; V<sub>IL</sub> (min.) = -2.0V AC (pulse width <10 ns). Not 100% tested.  
 V<sub>IH</sub> (max.) = V<sub>DD</sub> + 0.3V DC; V<sub>IH</sub> (max.) = V<sub>DD</sub> + 2.0V AC (pulse width <10 ns). Not 100% tested.

**DC ELECTRICAL CHARACTERISTICS** (Over Operating Range)

**V<sub>DD</sub> = 1.65V-2.2V**

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V <sub>OH</sub>	Output HIGH Voltage	V <sub>DD</sub> = Min, I <sub>OH</sub> = -0.1 mA	1.4	—	V
V <sub>OL</sub>	Output LOW Voltage	V <sub>DD</sub> = Min, I <sub>OL</sub> = 0.1 mA	—	0.2	V
V <sub>IH</sub>	Input HIGH Voltage		1.4	V <sub>DD</sub> + 0.2	V
V <sub>IL</sub> <sup>(1)</sup>	Input LOW Voltage		-0.2	0.4	V
I <sub>LI</sub>	Input Leakage	GND ≤ V <sub>IN</sub> ≤ V <sub>DD</sub>	-1	1	µA
I <sub>LO</sub>	Output Leakage	GND ≤ V <sub>OUT</sub> ≤ V <sub>DD</sub> , Outputs Disabled	-1	1	µA

**Note:**

1. V<sub>IL</sub> (min.) = -0.3V DC; V<sub>IL</sub> (min.) = -2.0V AC (pulse width <10 ns). Not 100% tested.  
 V<sub>IH</sub> (max.) = V<sub>DD</sub> + 0.3V DC; V<sub>IH</sub> (max.) = V<sub>DD</sub> + 2.0V AC (pulse width <10 ns). Not 100% tested.

### **ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

<b>Symbol</b>	<b>Parameter</b>	<b>Value</b>	<b>Unit</b>
V <sub>TERM</sub>	Terminal Voltage with Respect to GND	-0.5 to V <sub>DD</sub> + 0.5	V
V <sub>DD</sub>	V <sub>DD</sub> Relates to GND	-0.3 to 4.0	V
T <sub>TSG</sub>	Storage Temperature	-65 to +150	°C
P <sub>T</sub>	Power Dissipation	1.0	W

**Notes:**

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

### **CAPACITANCE<sup>(1,2)</sup>**

<b>Symbol</b>	<b>Parameter</b>	<b>Conditions</b>	<b>Max.</b>	<b>Unit</b>
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	6	pF
C <sub>I/O</sub>	Input/Output Capacitance	V <sub>OUT</sub> = 0V	8	pF

**Notes:**

1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T<sub>A</sub> = 25°C, f = 1 MHz, V<sub>DD</sub> = 3.3V.

## HIGH SPEED (IS61WV5128ALL/BLL)

### OPERATING RANGE ( $V_{DD}$ ) (IS61WV5128ALL)

Range	Ambient Temperature	$V_{DD}$	Speed
Commercial	0°C to +70°C	1.65V-2.2V	20ns
Industrial	-40°C to +85°C	1.65V-2.2V	20ns
Automotive	-40°C to +125°C	1.65V-2.2V	20ns

### OPERATING RANGE ( $V_{DD}$ ) (IS61WV5128BLL)<sup>(1)</sup>

Range	Ambient Temperature	$V_{DD}$ (8 ns) <sup>1</sup>	$V_{DD}$ (10 ns) <sup>1</sup>
Commercial	0°C to +70°C	3.3V $\pm$ 5%	2.4V-3.6V
Industrial	-40°C to +85°C	3.3V $\pm$ 5%	2.4V-3.6V

**Note:**

- When operated in the range of 2.4V-3.6V, the device meets 10ns. When operated in the range of 3.3V  $\pm$  5%, the device meets 8ns.

### OPERATING RANGE ( $V_{DD}$ ) (IS64WV5128BLL)

Range	Ambient Temperature	$V_{DD}$ (10 ns)
Automotive	-40°C to +125°C	2.4V-3.6V

### POWER SUPPLY CHARACTERISTICS<sup>(1)</sup> (Over Operating Range)

Symbol	Parameter	Test Conditions	-8		-10		-20		Unit	
			Min.	Max.	Min.	Max.	Min.	Max.		
Icc	V <sub>DD</sub> Dynamic Operating Supply Current	V <sub>DD</sub> = Max., I <sub>OUT</sub> = 0 mA, f = f <sub>MAX</sub>	Com.	—	50	—	40	—	40	mA
			Ind.	—	55	—	45	—	45	
			Auto.	—	—	—	65	—	65	
			typ. <sup>(2)</sup>			25				
Icc1	Operating Supply Current	V <sub>DD</sub> = Max., I <sub>OUT</sub> = 0 mA, f = 0	Com.	—	35	—	35	—	30	mA
			Ind.	—	40	—	40	—	40	
			Auto.	—	—	—	60	—	60	
Isb1	TTL Standby Current (TTL Inputs)	V <sub>DD</sub> = Max., V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> , CE $\geq$ V <sub>IH</sub> , f = 0	Com.	—	10	—	10	—	10	mA
			Ind.	—	15	—	15	—	15	
			Auto.	—	—	—	30	—	30	
Isb2	CMOS Standby Current (CMOS Inputs)	V <sub>DD</sub> = Max., CE $\geq$ V <sub>DD</sub> - 0.2V, V <sub>IN</sub> $\geq$ V <sub>DD</sub> - 0.2V, or V <sub>IN</sub> $\leq$ 0.2V, f = 0	Com.	—	6	—	6	—	6	mA
			Ind.	—	8	—	8	—	8	
			Auto.	—	—	—	15	—	15	
			typ. <sup>(2)</sup>			2				

**Note:**

- At f = f<sub>MAX</sub>, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.
- Typical values are measured at V<sub>DD</sub> = 3.0V, T<sub>A</sub> = 25°C and not 100% tested.

## LOW POWER (IS61WV5128ALS/BLS)

### OPERATING RANGE (V<sub>DD</sub>) (IS61WV5128ALS)

Range	Ambient Temperature	V <sub>DD</sub>	Speed
Commercial	0°C to +70°C	1.65V-2.2V	35ns
Industrial	-40°C to +85°C	1.65V-2.2V	35ns
Automotive	-40°C to +125°C	1.65V-2.2V	35ns

### OPERATING RANGE (V<sub>DD</sub>) (IS61WV5128BLS)<sup>(1)</sup>

Range	Ambient Temperature	V <sub>DD</sub>	Speed
Commercial	0°C to +70°C	2.4V-3.6V	25 ns
Industrial	-40°C to +85°C	2.4V-3.6V	25 ns

### OPERATING RANGE (V<sub>DD</sub>) (IS64WV5128BLS)

Range	Ambient Temperature	V <sub>DD</sub>	Speed
Automotive	-40°C to +125°C	2.4V-3.6V	35 ns

### POWER SUPPLY CHARACTERISTICS<sup>(1)</sup> (Over Operating Range)

Symbol	Parameter	Test Conditions	-25		-35		Unit	
			Min.	Max.	Min.	Max.		
Icc	V <sub>DD</sub> Dynamic Operating Supply Current	V <sub>DD</sub> = Max., I <sub>OUT</sub> = 0 mA, f = f <sub>MAX</sub>	Com.	—	20	—	20	mA
			Ind.	—	25	—	25	
			Auto.	—	50	—	50	
			typ. <sup>(2)</sup>	11				
Icc1	Operating Supply Current	V <sub>DD</sub> = Max., I <sub>OUT</sub> = 0 mA, f = 0	Com.	—	10	—	10	mA
			Ind.	—	12	—	12	
			Auto.	—	20	—	20	
Isb1	TTL Standby Current (TTL Inputs)	V <sub>DD</sub> = Max., V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> , $\overline{CE} \geq V_{IH}$ , f = 0	Com.	—	5	—	5	mA
			Ind.	—	7	—	7	
			Auto.	—	10	—	10	
Isb2	CMOS Standby Current (CMOS Inputs)	V <sub>DD</sub> = Max., $\overline{CE} \geq V_{DD} - 0.2V$ , V <sub>IN</sub> ≥ V <sub>DD</sub> - 0.2V, or V <sub>IN</sub> ≤ 0.2V, f = 0	Com.	—	1	—	1	mA
			Ind.	—	2	—	2	
			Auto.	—	10	—	10	
			typ. <sup>(2)</sup>	0.2				

**Note:**

- At f = f<sub>MAX</sub>, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.
- Typical values are measured at V<sub>DD</sub> = 3.0V, T<sub>A</sub> = 25°C and not 100% tested.

## AC TEST CONDITIONS

Parameter	Unit (2.4V-3.6V)	Unit (3.3V ± 10%)	Unit (1.65V-2.2V)
Input Pulse Level	0V to 3V	0V to 3V	0V to 1.8V
Input Rise and Fall Times	1V/ ns	1V/ ns	1V/ ns
Input and Output Timing and Reference Level ( $V_{Ref}$ )	1.5V	1.5V	0.9V
Output Load	See Figures 1 and 2	See Figures 1 and 2	See Figures 1 and 2

## AC TEST LOADS

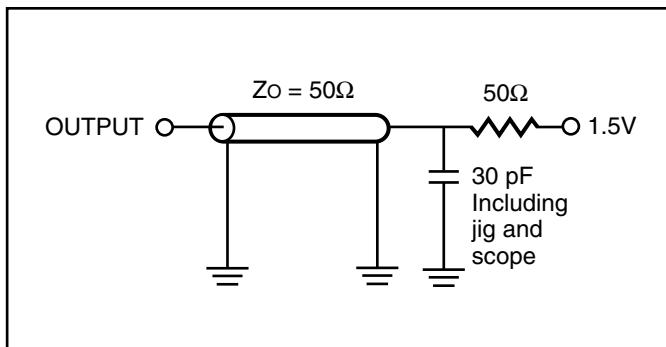


Figure 1.

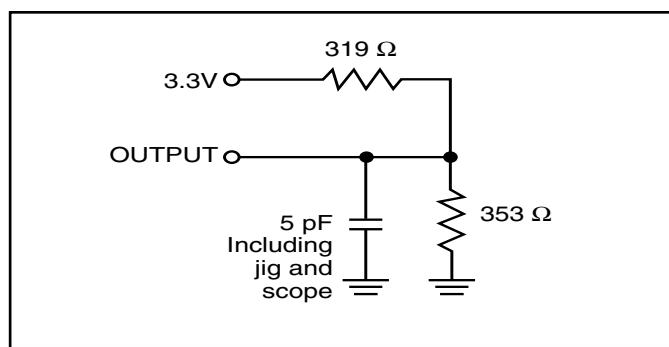


Figure 2.

**READ CYCLE SWITCHING CHARACTERISTICS<sup>(1)</sup> (Over Operating Range)**

Symbol	Parameter	<b>-8</b>		<b>-10</b>		Unit
		Min.	Max.	Min.	Max.	
t <sub>RC</sub>	Read Cycle Time	8	—	10	—	ns
t <sub>AA</sub>	Address Access Time	—	8	—	10	ns
t <sub>OH</sub>	Output Hold Time	2.0	—	2.0	—	ns
t <sub>ACE</sub>	CE Access Time	—	8	—	10	ns
t <sub>DOE</sub>	OE Access Time	—	4.5	—	4.5	ns
t <sub>HZOE</sub> <sup>(2)</sup>	OE to High-Z Output	—	3	—	4	ns
t <sub>LZOE</sub> <sup>(2)</sup>	OE to Low-Z Output	0	—	0	—	ns
t <sub>HZCE</sub> <sup>(2)</sup>	CE to High-Z Output	0	3	0	4	ns
t <sub>LZCE</sub> <sup>(2)</sup>	CE to Low-Z Output	3	—	3	—	ns
t <sub>PU</sub>	Power Up Time	0	—	0	—	ns
t <sub>PD</sub>	Power Down Time	—	8	—	10	ns

**Notes:**

1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0V to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage.

READ CYCLE SWITCHING CHARACTERISTICS<sup>(1)</sup> (Over Operating Range)

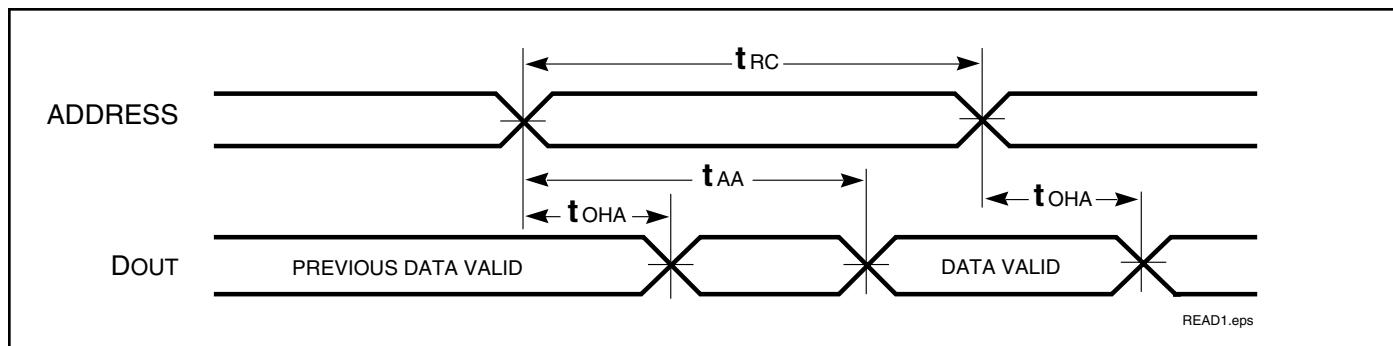
<b>Symbol</b>	<b>Parameter</b>	<b>-20 ns</b>		<b>-25 ns</b>		<b>-35 ns</b>		<b>Unit</b>
		<b>Min.</b>	<b>Max.</b>	<b>Min.</b>	<b>Max.</b>	<b>Min.</b>	<b>Max.</b>	
t <sub>RC</sub>	Read Cycle Time	20	—	25	—	35	—	ns
t <sub>AA</sub>	Address Access Time	—	20	—	25	—	35	ns
t <sub>TOHA</sub>	Output Hold Time	2.5	—	4	—	4	—	ns
t <sub>TACE</sub>	CE Access Time	—	20	—	25	—	35	ns
t <sub>TDOE</sub>	OE Access Time	—	8	—	12	—	15	ns
t <sub>THZOE</sub> <sup>(2)</sup>	OE to High-Z Output	0	8	0	8	0	10	ns
t <sub>TLZOE</sub> <sup>(2)</sup>	OE to Low-Z Output	0	—	0	—	0	—	ns
t <sub>THZCE</sub> <sup>(2)</sup>	CE to High-Z Output	0	8	0	8	0	10	ns
t <sub>TLZCE</sub> <sup>(2)</sup>	CE to Low-Z Output	3	—	10	—	10	—	ns
t <sub>TPU</sub>	Power Up Time	0	—	0	—	0	—	ns
t <sub>PD</sub>	Power Down Time	—	20	—	25	—	35	ns

**Notes:**

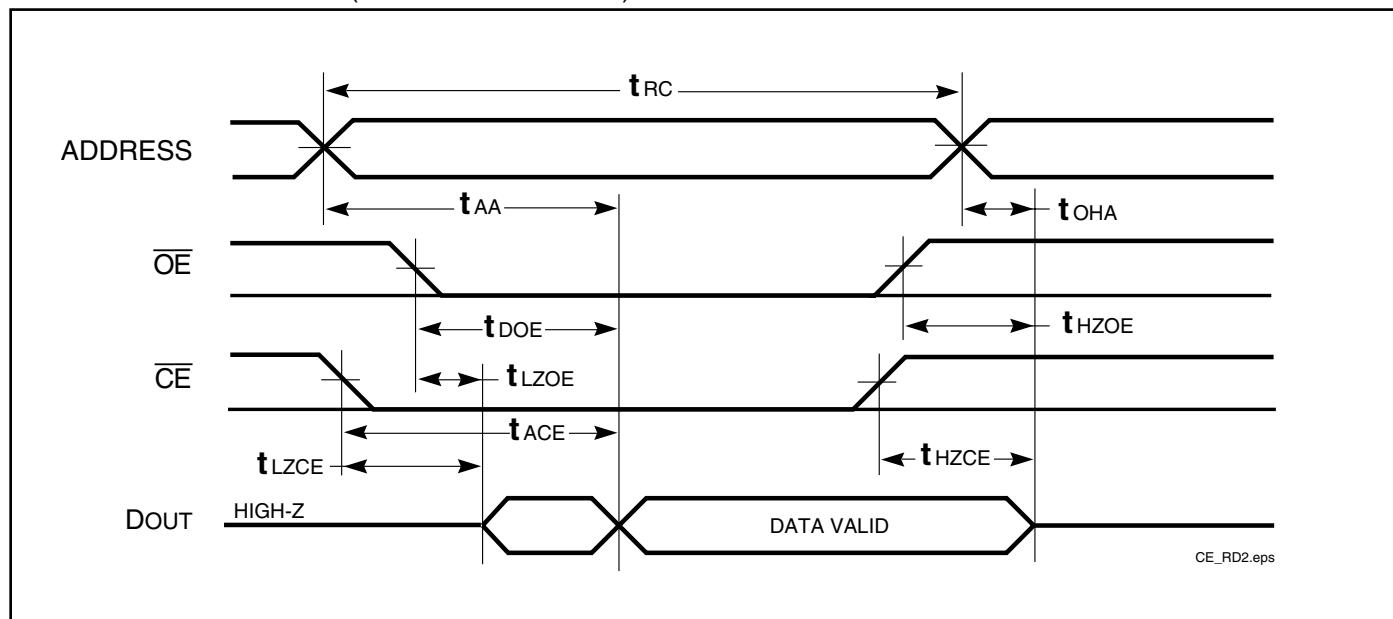
1. Test conditions assume signal transition times of 1.5 ns or less, timing reference levels of 1.25V, input pulse levels of 0.4V to V<sub>DD</sub>-0.3V and output loading specified in Figure 1a.
2. Tested with the load in Figure 1b. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.
3. Not 100% tested.

## AC WAVEFORMS

**READ CYCLE NO. 1<sup>(1,2)</sup>** (Address Controlled) ( $\overline{CE} = \overline{OE} = V_{IL}$ )



**READ CYCLE NO. 2<sup>(1,3)</sup>** ( $\overline{CE}$  and  $\overline{OE}$  Controlled)



### Notes:

1.  $\overline{WE}$  is HIGH for a Read Cycle.
2. The device is continuously selected.  $\overline{OE}, \overline{CE} = V_{IL}$ .
3. Address is valid prior to or coincident with  $\overline{CE}$  LOW transitions.

**WRITE CYCLE SWITCHING CHARACTERISTICS<sup>(1,3)</sup> (Over Operating Range)**

Symbol	Parameter	-8		-10		Unit
		Min.	Max.	Min.	Max.	
t <sub>WC</sub>	Write Cycle Time	8	—	10	—	ns
t <sub>SCE</sub>	CE to Write End	6.5	—	8	—	ns
t <sub>AW</sub>	Address Setup Time to Write End	6.5	—	8	—	ns
t <sub>HA</sub>	Address Hold from Write End	0	—	0	—	ns
t <sub>SA</sub>	Address Setup Time	0	—	0	—	ns
t <sub>PWE1</sub>	WE Pulse Width ( $\overline{OE} = \text{HIGH}$ )	6.5	—	8	—	ns
t <sub>PWE2</sub>	WE Pulse Width ( $\overline{OE} = \text{LOW}$ )	8.0	—	10	—	ns
t <sub>SD</sub>	Data Setup to Write End	5	—	6	—	ns
t <sub>HD</sub>	Data Hold from Write End	0	—	0	—	ns
t <sub>HZWE<sup>(2)</sup></sub>	WE LOW to High-Z Output	—	3.5	—	5	ns
t <sub>LZWE<sup>(2)</sup></sub>	WE HIGH to Low-Z Output	2	—	2	—	ns

**Notes:**

1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0V to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured  $\pm 500$  mV from steady-state voltage. Not 100% tested.
3. The internal write time is defined by the overlap of CE LOW and WE LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write. Shaded area product in development

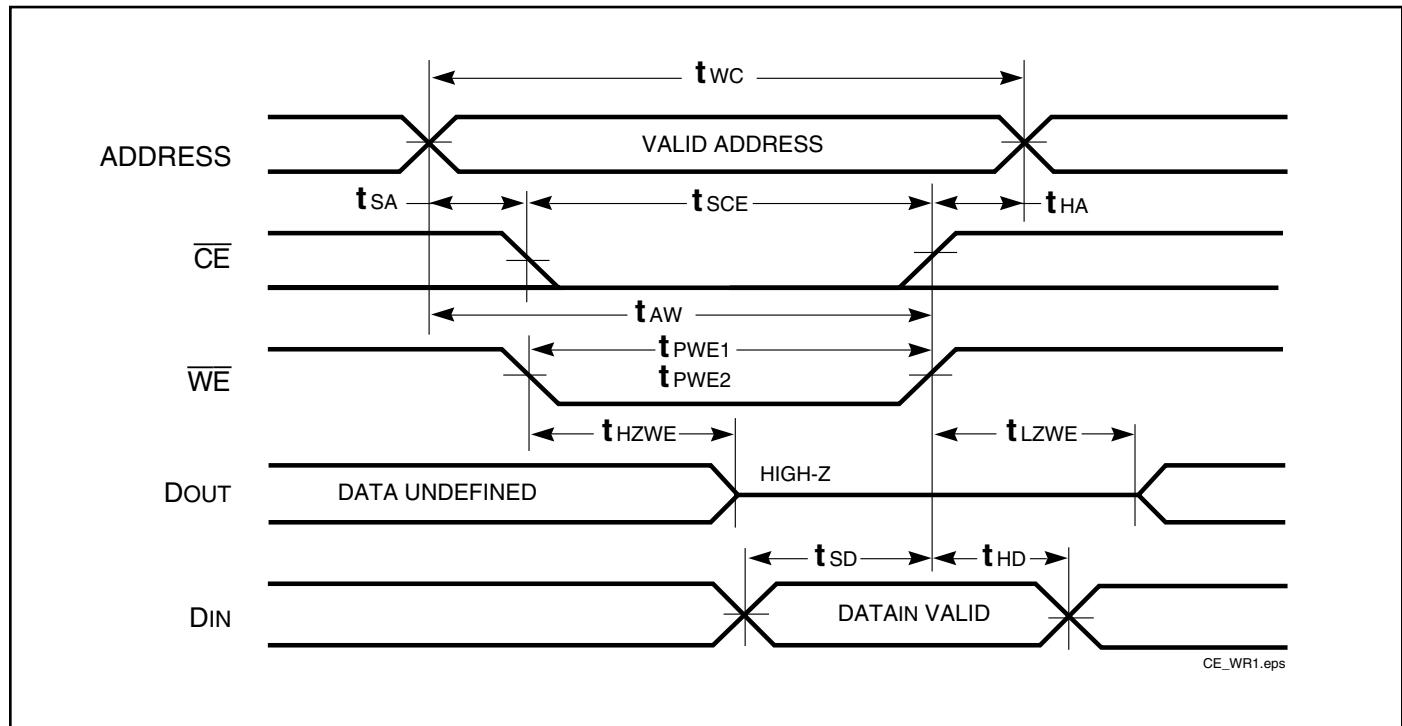
**WRITE CYCLE SWITCHING CHARACTERISTICS<sup>(1,2)</sup> (Over Operating Range)**

Symbol	Parameter	-20 ns		-25 ns		-35 ns		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>WC</sub>	Write Cycle Time	20	—	25	—	35	—	ns
t <sub>SCE</sub>	CE to Write End	12	—	18	—	25	—	ns
t <sub>AW</sub>	Address Setup Time to Write End	12	—	15	—	25	—	ns
t <sub>HA</sub>	Address Hold from Write End	0	—	0	—	0	—	ns
t <sub>SA</sub>	Address Setup Time	0	—	0	—	0	—	ns
t <sub>PWE1</sub>	WE Pulse Width (OE = HIGH)	12	—	18	—	30	—	ns
t <sub>PWE2</sub>	WE Pulse Width (OE = LOW)	17	—	20	—	30	—	ns
t <sub>SD</sub>	Data Setup to Write End	9	—	12	—	15	—	ns
t <sub>HD</sub>	Data Hold from Write End	0	—	0	—	0	—	ns
t <sub>HZWE<sup>(3)</sup></sub>	WE LOW to High-Z Output	—	9	—	12	—	20	ns
t <sub>LZWE<sup>(3)</sup></sub>	WE HIGH to Low-Z Output	3	—	5	—	5	—	ns

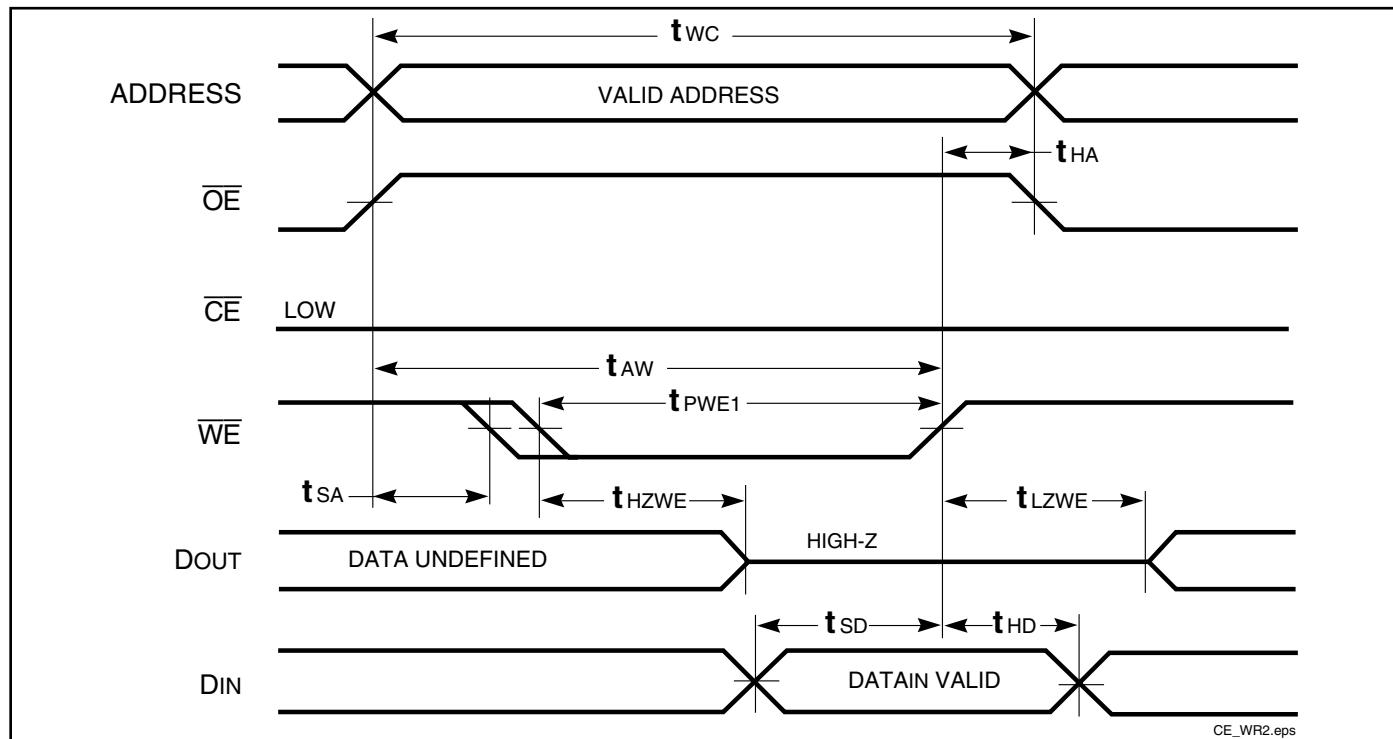
**Notes:**

1. Test conditions for IS61WV6416LL assume signal transition times of 1.5ns or less, timing reference levels of 1.25V, input pulse levels of 0.4V to V<sub>DD</sub>-0.3V and output loading specified in Figure 1a.
2. Tested with the load in Figure 1b. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.
3. The internal write time is defined by the overlap of CE LOW and WE LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.

## AC WAVEFORMS

WRITE CYCLE NO. 1<sup>(1,2)</sup> ( $\overline{CE}$  Controlled,  $\overline{OE}$  = HIGH or LOW)

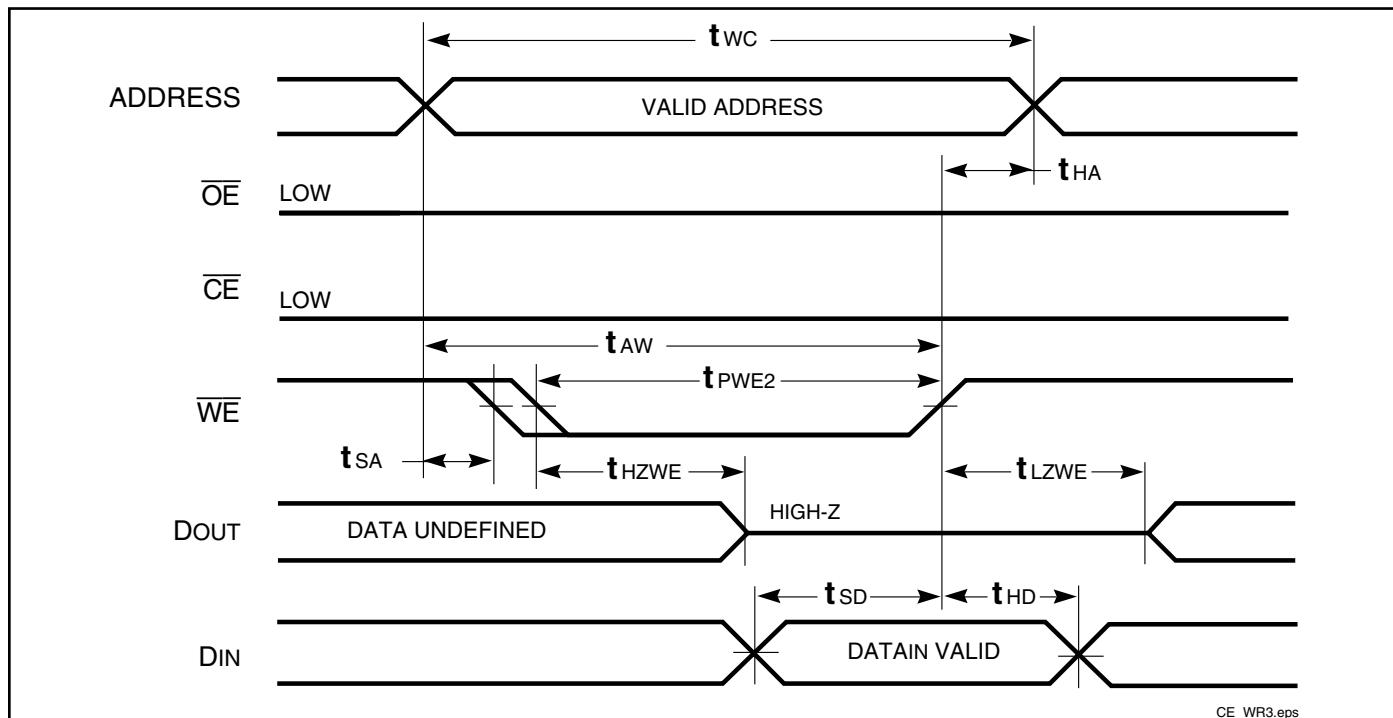
**WRITE CYCLE NO. 2<sup>(1,2)</sup> ( $\overline{WE}$  Controlled:  $\overline{OE}$  is HIGH During Write Cycle)**



**Notes:**

1. The internal write time is defined by the overlap of  $\overline{CE}$  LOW and  $\overline{WE}$  LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
2. I/O will assume the High- $Z$  state if  $\overline{OE} > V_{IH}$ .

**WRITE CYCLE NO. 3 ( $\overline{WE}$  Controlled:  $\overline{OE}$  is LOW During Write Cycle)**



## HIGH SPEED (IS61WV5128ALL/BLL)

### DATA RETENTION SWITCHING CHARACTERISTICS (2.4V-3.6V)

Symbol	Parameter	Test Condition	Options	Min.	Typ. <sup>(1)</sup>	Max.	Unit
$V_{DR}$	V <sub>DD</sub> for Data Retention	See Data Retention Waveform		2.0	—	3.6	V
$I_{DR}$	Data Retention Current	$V_{DD} = 2.0V, \overline{CE} \geq V_{DD} - 0.2V$	Com.	—	2	6	mA
			Ind.	—	—	8	
			Auto.			15	
$t_{SDR}$	Data Retention Setup Time	See Data Retention Waveform		0	—	—	ns
$t_{RDR}$	Recovery Time	See Data Retention Waveform		$t_{RC}$	—	—	ns

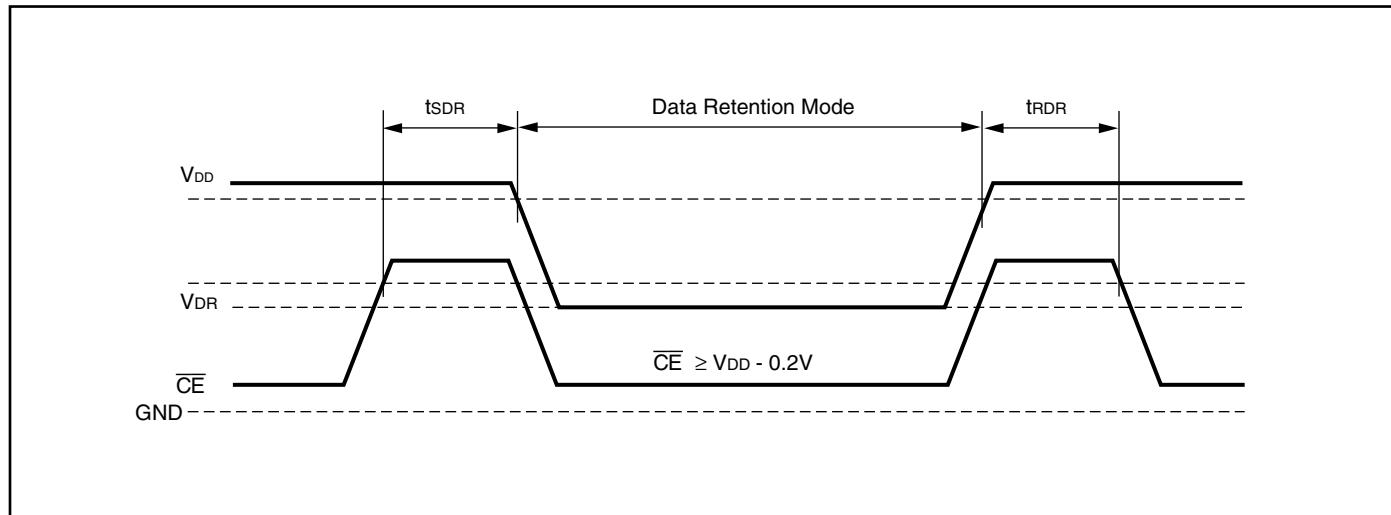
Note 1: Typical values are measured at  $V_{DD} = 3.0V$ ,  $T_A = 25^\circ C$  and not 100% tested.

### DATA RETENTION SWITCHING CHARACTERISTICS (1.65V-2.2V)

Symbol	Parameter	Test Condition	Options	Min.	Typ. <sup>(1)</sup>	Max.	Unit
$V_{DR}$	V <sub>DD</sub> for Data Retention	See Data Retention Waveform		1.2	—	3.6	V
$I_{DR}$	Data Retention Current	$V_{DD} = 1.2V, \overline{CE} \geq V_{DD} - 0.2V$	Com.	—	2	6	mA
			Ind.	—	—	8	
$t_{SDR}$	Data Retention Setup Time	See Data Retention Waveform		0	—	—	ns
$t_{RDR}$	Recovery Time	See Data Retention Waveform		$t_{RC}$	—	—	ns

Note 1: Typical values are measured at  $V_{DD} = 1.8V$ ,  $T_A = 25^\circ C$  and not 100% tested.

### DATA RETENTION WAVEFORM ( $\overline{CE}$ Controlled)



## LOW POWER (IS61WV5128ALS/BLS)

### DATA RETENTION SWITCHING CHARACTERISTICS (2.4V-3.6V)

Symbol	Parameter	Test Condition	Options	Min.	Typ. <sup>(1)</sup>	Max.	Unit
V <sub>DR</sub>	V <sub>DD</sub> for Data Retention	See Data Retention Waveform		2.0	—	3.6	V
I <sub>DR</sub>	Data Retention Current	V <sub>DD</sub> = 2.0V, $\overline{CE} \geq V_{DD} - 0.2V$	Com.	—	0.2	1	mA
			Ind.	—	—	2	
			Auto.			10	
t <sub>SDR</sub>	Data Retention Setup Time	See Data Retention Waveform		0	—	—	ns
t <sub>RDRA</sub>	Recovery Time	See Data Retention Waveform	t <sub>RC</sub>	—	—	—	ns

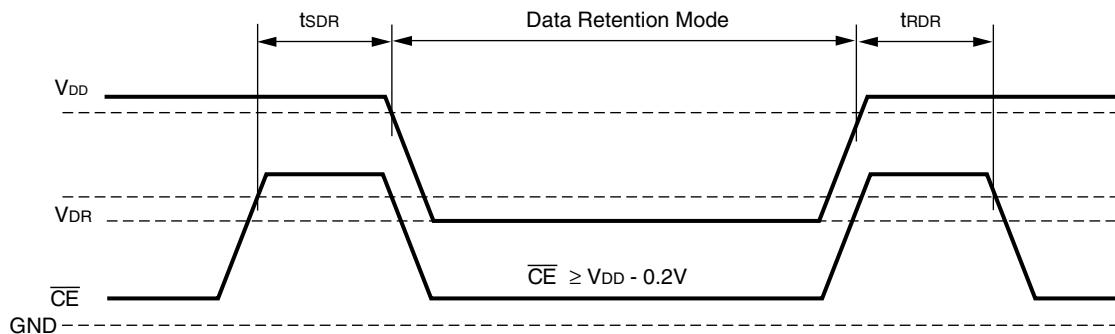
**Note 1:** Typical values are measured at V<sub>DD</sub> = 3.0V, T<sub>A</sub> = 25°C and not 100% tested.

### DATA RETENTION SWITCHING CHARACTERISTICS (1.65V-2.2V)

Symbol	Parameter	Test Condition	Options	Min.	Typ. <sup>(1)</sup>	Max.	Unit
V <sub>DR</sub>	V <sub>DD</sub> for Data Retention	See Data Retention Waveform		1.2	—	3.6	V
I <sub>DR</sub>	Data Retention Current	V <sub>DD</sub> = 1.2V, $\overline{CE} \geq V_{DD} - 0.2V$	Com.	—	0.2	1	mA
			Ind.	—	—	2	
t <sub>SDR</sub>	Data Retention Setup Time	See Data Retention Waveform		0	—	—	ns
t <sub>RDRA</sub>	Recovery Time	See Data Retention Waveform	t <sub>RC</sub>	—	—	—	ns

**Note 1:** Typical values are measured at V<sub>DD</sub> = 1.8V, T<sub>A</sub> = 25°C and not 100% tested.

### DATA RETENTION WAVEFORM ( $\overline{CE}$ Controlled)



**IS61WV5128ALL/ALS, IS61WV5128BLL/BLS  
IS64WV5128BLL/BLS**

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**ORDERING INFORMATION (HIGH SPEED)**

**Commercial Range: 0°C to +70°C**

**Voltage Range: 2.4V to 3.6V**

Speed (ns)	Order Part No.	Package
10 (8 <sup>1</sup> )	IS61WV5128BLL-10TL	TSOP (Type II), Lead-free

**Note:**

1. Speed = 8ns for V<sub>DD</sub> = 3.3V ± 5%. Speed = 10ns for V<sub>DD</sub> = 2.4V to 3.3V.

**Industrial Range: -40°C to +85°C**

**Voltage Range: 2.4V to 3.6V**

Speed (ns)	Order Part No.	Package
10 (8 <sup>1</sup> )	IS61WV5128BLL-10BI	36-ball mini BGA (6mm x 8mm)
	IS61WV5128BLL-10BLI	36-ball mini BGA (6mm x 8mm), Lead-free
	IS61WV5128BLL-10TI	TSOP (Type II)
	IS61WV5128BLL-10TLI	TSOP (Type II), Lead-free
	IS61WV5128BLL-10KLI	400-mil Plastic SOJ, Lead-free

**Note:**

1. Speed = 8ns for V<sub>DD</sub> = 3.3V ± 5%. Speed = 10ns for V<sub>DD</sub> = 2.4V to 3.3V.

**Industrial Range: -40°C to +85°C**

**Voltage Range: 1.65V to 2.2V**

Speed (ns)	Order Part No.	Package
20	IS61WV5128ALL-20BI	36-ball mini BGA (6mm x 8mm)
	IS61WV5128ALL-20TI	TSOP (Type II)

**Automotive Range: -40°C to +125°C**

**Voltage Range: 2.4V to 3.6V**

Speed (ns)	Order Part No.	Package
10	IS64WV5128BLL-10BA3	36-ball mini BGA (6mm x 8mm)
	IS64WV5128BLL-10TA3	TSOP (Type II)

**ORDERING INFORMATION (LOW POWER)**

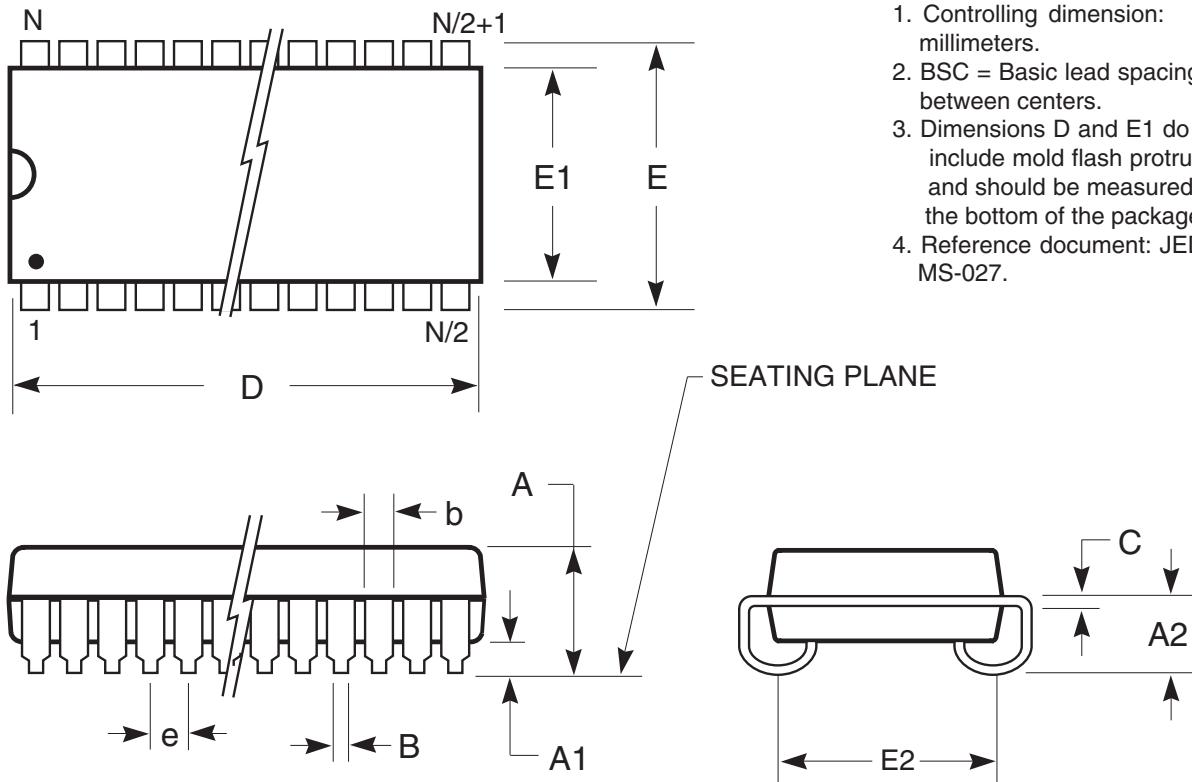
**Industrial Range: -40°C to +125°C**

**Voltage Range: 2.4V to 3.6V**

Speed (ns)	Order Part No.	Package
25	IS61WV5128BLS-25TLI	TSOP (Type II), Lead-free

# PACKAGING INFORMATION

400-mil Plastic SOJ  
Package Code: K



## Notes:

1. Controlling dimension: millimeters.
2. BSC = Basic lead spacing between centers.
3. Dimensions D and E1 do not include mold flash protrusions and should be measured from the bottom of the package.
4. Reference document: JEDEC MS-027.

Symbol	Millimeters		Inches		Millimeters		Inches		Millimeters		Inches	
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
No. Leads (N)	28		32		36							
A	3.25	3.75	0.128	0.148	3.25	3.75	0.128	0.148	3.25	3.75	0.128	0.148
A1	0.64	—	0.025	—	0.64	—	0.025	—	0.64	—	0.025	—
A2	2.08	—	0.082	—	2.08	—	0.082	—	2.08	—	0.082	—
B	0.38	0.51	0.015	0.020	0.38	0.51	0.015	0.020	0.38	0.51	0.015	0.020
b	0.66	0.81	0.026	0.032	0.66	0.81	0.026	0.032	0.66	0.81	0.026	0.032
C	0.18	0.33	0.007	0.013	0.18	0.33	0.007	0.013	0.18	0.33	0.007	0.013
D	18.29	18.54	0.720	0.730	20.82	21.08	0.820	0.830	23.37	23.62	0.920	0.930
E	11.05	11.30	0.435	0.445	11.05	11.30	0.435	0.445	11.05	11.30	0.435	0.445
E1	10.03	10.29	0.395	0.405	10.03	10.29	0.395	0.405	10.03	10.29	0.395	0.405
E2	9.40 BSC		0.370 BSC		9.40 BSC		0.370 BSC		9.40 BSC		0.370 BSC	
e	1.27 BSC		0.050 BSC		1.27 BSC		0.050 BSC		1.27 BSC		0.050 BSC	

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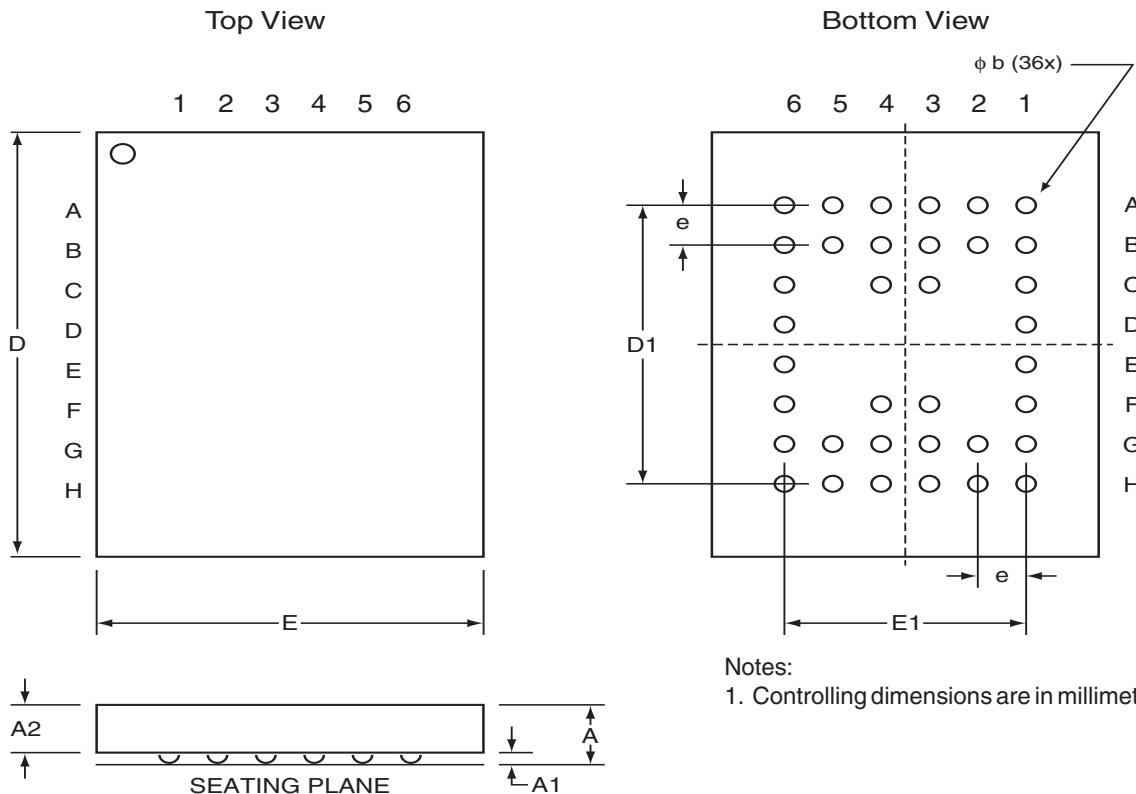
# PACKAGING INFORMATION

Symbol	Millimeters		Inches		Millimeters		Inches		Millimeters		Inches	
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
No. Leads (N)	40				42				44			
A	3.25	3.75	0.128	0.148	3.25	3.75	0.128	0.148	3.25	3.75	0.128	0.148
A1	0.64	—	0.025	—	0.64	—	0.025	—	0.64	—	0.025	—
A2	2.08	—	0.082	—	2.08	—	0.082	—	2.08	—	0.082	—
B	0.38	0.51	0.015	0.020	0.38	0.51	0.015	0.020	0.38	0.51	0.015	0.020
b	0.66	0.81	0.026	0.032	0.66	0.81	0.026	0.032	0.66	0.81	0.026	0.032
C	0.18	0.33	0.007	0.013	0.18	0.33	0.007	0.013	0.18	0.33	0.007	0.013
D	25.91	26.16	1.020	1.030	27.18	27.43	1.070	1.080	28.45	28.70	1.120	1.130
E	11.05	11.30	0.435	0.445	11.05	11.30	0.435	0.445	11.05	11.30	0.435	0.445
E1	10.03	10.29	0.395	0.405	10.03	10.29	0.395	0.405	10.03	10.29	0.395	0.405
E2	9.40 BSC		0.370 BSC		9.40 BSC		0.370 BSC		9.40 BSC		0.370 BSC	
e	1.27 BSC		0.050 BSC		1.27 BSC		0.050 BSC		1.27 BSC		0.050 BSC	

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# PACKAGING INFORMATION

**Mini Ball Grid Array**  
**Package Code: B (36-pin)**



Notes:

1. Controlling dimensions are in millimeters.

## mBGA - 6mm x 8mm

	MILLIMETERS			INCHES		
Sym.	Min.	Typ.	Max.	Min.	Typ.	Max.
NO.						
Leads	<b>36</b>			<b>36</b>		
A	—	—	1.20	—	—	0.047
A1	0.24	—	0.30	0.009	—	0.012
A2	0.60	—	—	0.024	—	—
D	7.90	8.00	8.10	0.311	0.315	0.319
D1	5.25BSC			0.207BSC		
E	5.90	6.00	6.10	0.232	0.236	0.240
E1	3.75BSC			0.148BSC		
e	0.75BSC			0.030BSC		
b	0.30	0.35	0.40	0.012	0.014	0.016

## mBGA - 8mm x 10mm

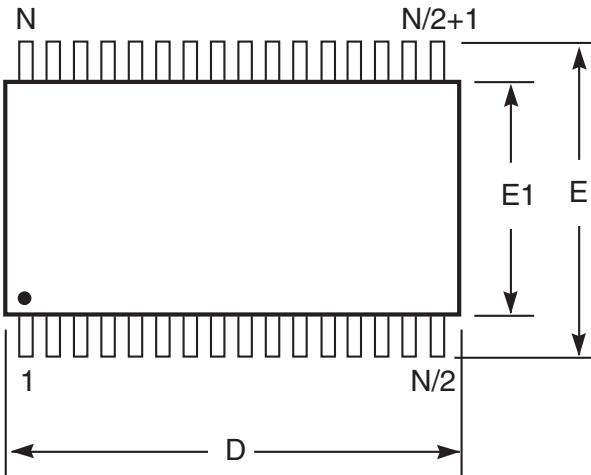
	MILLIMETER			INCHES		
Sym.	Min.	Typ.	Max.	Min.	Typ.	Max.
NO.						
Leads	<b>36</b>			<b>36</b>		
A	—	—	1.20	—	—	0.047
A1	0.24	—	0.30	0.009	—	0.012
A2	0.60	—	—	0.024	—	—
D	9.90	10.00	10.10	0.390	0.394	0.398
D1	5.25BSC			0.207BSC		
E	7.90	8.00	8.10	0.311	0.315	0.319
E1	3.75BSC			0.148BSC		
e	0.75BSC			0.030BSC		
b	0.30	0.35	0.40	0.012	0.014	0.016

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# PACKAGING INFORMATION

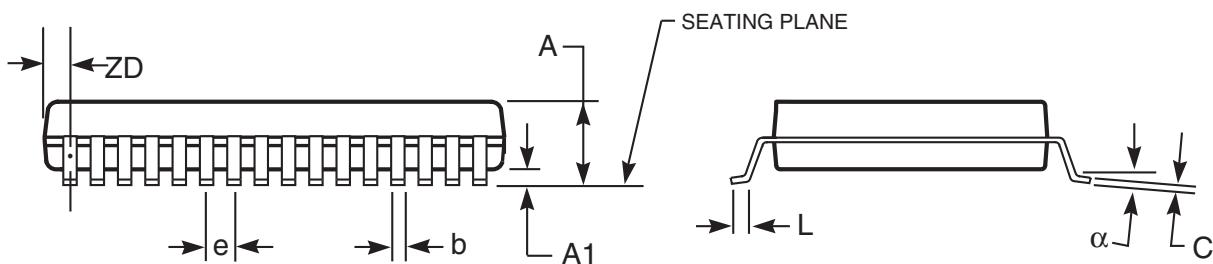
Plastic TSOP

Package Code: T (Type II)



**Notes:**

1. Controlling dimension: millimeters, unless otherwise specified.
2. BSC = Basic lead spacing between centers.
3. Dimensions D and E1 do not include mold flash protrusions and should be measured from the bottom of the package.
4. Formed leads shall be planar with respect to one another within 0.004 inches at the seating plane.



Plastic TSOP (T - Type II)

Symbol	Millimeters		Inches		Millimeters		Inches		Millimeters		Inches	
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
Ref. Std.												
No. Leads (N)	32				44				50			
A	—	1.20	—	0.047	—	1.20	—	0.047	—	1.20	—	0.047
A1	0.05	0.15	0.002	0.006	0.05	0.15	0.002	0.006	0.05	0.15	0.002	0.006
b	0.30	0.52	0.012	0.020	0.30	0.45	0.012	0.018	0.30	0.45	0.012	0.018
C	0.12	0.21	0.005	0.008	0.12	0.21	0.005	0.008	0.12	0.21	0.005	0.008
D	20.82	21.08	0.820	0.830	18.31	18.52	0.721	0.729	20.82	21.08	0.820	0.830
E1	10.03	10.29	0.391	0.400	10.03	10.29	0.395	0.405	10.03	10.29	0.395	0.405
E	11.56	11.96	0.451	0.466	11.56	11.96	0.455	0.471	11.56	11.96	0.455	0.471
e	1.27	BSC	0.050	BSC	0.80	BSC	0.032	BSC	0.80	BSC	0.031	BSC
L	0.40	0.60	0.016	0.024	0.41	0.60	0.016	0.024	0.40	0.60	0.016	0.024
ZD	0.95 REF		0.037 REF		0.81 REF		0.032 REF		0.88 REF		0.035 REF	
$\alpha$	0°	5°	0°	5°	0°	5°	0°	5°	0°	5°	0°	5°

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