

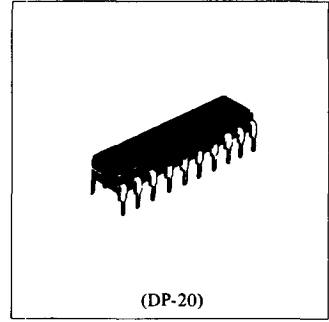
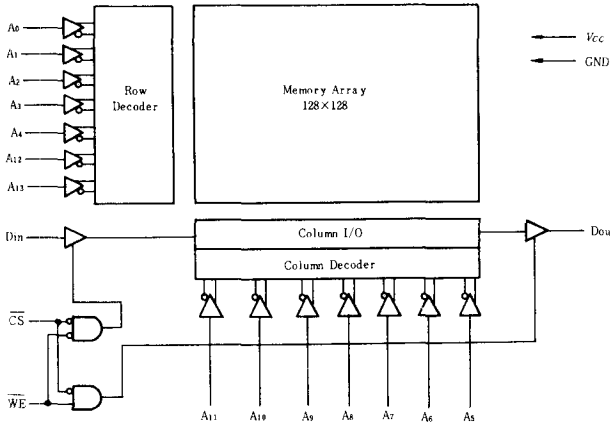
HM6167HLP-45, HM6167HLP-55

16384-word x 1-bit High Speed Static CMOS RAM

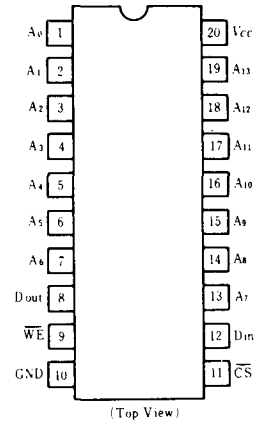
■ FEATURES

- Fast Access Time.HM6167HLP-45 45ns (max)
HM6167HLP-55 55ns (max)
- Low Power Standby and Low Power Operation
Standby $5\mu\text{W}$ (typ) and Operating 200mW (typ)
- Capable of Battery Back-up Operation
- Single +5V Supply and High Density 20 Pin Package
- Completely static Memory
No Clock or Timing Strobe Required
- Equal Access and Cycle Times
- Directly TTL CompatibleAll Inputs and Output

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Terminal Voltage with respect to GND	V_T	-3.5* to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	-55 to +125	°C
Storage Temperature Under Bias	T_{bias}	-10 to +85	°C

* Pulse Width 20ns, DC: -0.5V

■ RECOMMENDED DC OPERATING CONDITIONS ($T_a = 0$ to +70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input Voltage	V_{IH}	2.2	-	6.0	V
	V_{IL}	-3.0*	-	0.8	V

* Pulse Width 20ns, DC: V_{IL} min = -0.5V

TRUTH TABLE

\overline{CS}	\overline{WE}	Mode	V_{CC} Current	Dout Pin	Ref. Cycle
H	x	Not selected	I_{SA}, I_{SB1}	High-Z	
L	H	Read	I_{CC}	Dout	Read Cycle
L	L	Write	I_{CC}	High-Z	Write Cycle

DC AND OPERATING CHARACTERISTICS ($V_{CC}=5V \pm 10\%$, $T_a=0 \sim +70^\circ C$)

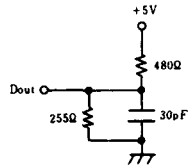
Item	Symbol	Test Conditions	min	typ	max	Unit
Input Leakage Current	$ I_{LI} $	$V_{CC}=5.5V$ $V_{IN}=0V \sim V_{CC}$	—	—	2	μA
Output Leakage Current	$ I_{LO} $	$\overline{CS}=V_{IN}$, $V_{OUT}=0V \sim V_{CC}$	—	—	2	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}=V_{IL}$, Output Open	—	40	80	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}=V_{IN}$	—	10	20	mA
	I_{SB1}	$\overline{CS}=V_{CC}-0.2V$ $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC}-0.2V$	—	1	50	μA
Output Low Voltage	V_{OL}	$I_{OL}=8mA$	—	—	0.4	V
Output High Voltage	V_{OH}	$I_{OH}=-4mA$	2.4	—	—	V

Note) Typical limits are at $V_{CC}=5.0V$, $T_a=25^\circ C$ and specified loading.

AC TEST CONDITIONS

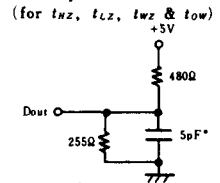
Input pulse levels: GND to 3.0V
 Input rise and fall times: 5 ns
 Input timing reference levels: 1.5V
 Output reference levels: 1.5V
 Output load: See Figure

Output Load A



* Including scope and jig.

Output Load B



* Including scope and jig.

CAPACITANCE ($T_a=25^\circ C$, $f=1MHz$)

Item	Symbol	typ.	max	Unit	Conditions
Input Capacitance	C_{IN}	3	5	pF	$V_{IN}=0V$
Output Capacitance	C_{OUT}	5	7	pF	$V_{OUT}=0V$

Note) This parameter is sampled and not 100% tested.

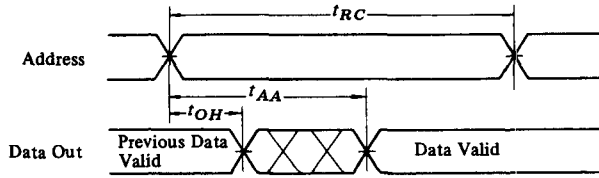
AC CHARACTERISTICS ($T_a=0^\circ C$ to $+70^\circ C$, $V_{CC}=5V \pm 10\%$, unless otherwise noted.)

READ CYCLE

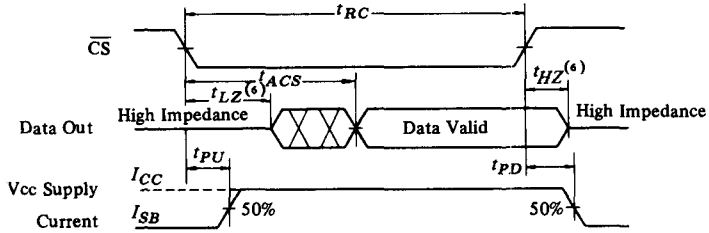
Item	Symbol	HM6167HLP-45		HM6167HLP-55		Unit	Notes
		min	max	min	max		
Read Cycle Time	t_{RC}	45	—	55	—	ns	(1)
Address Access Time	t_{AA}	—	45	—	55	ns	
Chip Select Access Time	t_{ACS}	—	45	—	55	ns	
Output Hold from Address Change	t_{OH}	5	—	5	—	ns	
Chip Selection to Output in Low Z	t_{LZ}	5	—	5	—	ns	(2) (3) (7)
Chip Selection to Output in High Z	t_{HZ}	0	30	0	30	ns	(2) (3) (7)
Chip Selection to Power Up Time	t_{PU}	0	—	0	—	ns	
Chip Deselection to Power Down Time	t_{PD}	—	30	—	30	ns	

- NOTES: 1. All Read Cycle timing are referenced from last valid address to the first transitioning address.
 2. At any given temperature and voltage condition, t_{HZ} max. is less than t_{LZ} min. both for a given device and from device to device.
 3. Transition is measured $\pm 500mV$ from steady state voltage with specified loading in Load B.
 4. \overline{WE} is High for READ cycle.
 5. Device is continuously selected, $\overline{CS}=V_{IL}$.
 6. Addresses valid prior to or coincident with \overline{CS} transition low.
 7. This parameter is sampled and not 100% tested.

●TIMING WAVEFORM OF READ CYCLE NO. 1 (4) 5)



●TIMING WAVEFORM OF READ CYCLE NO. 2 (4) 6)

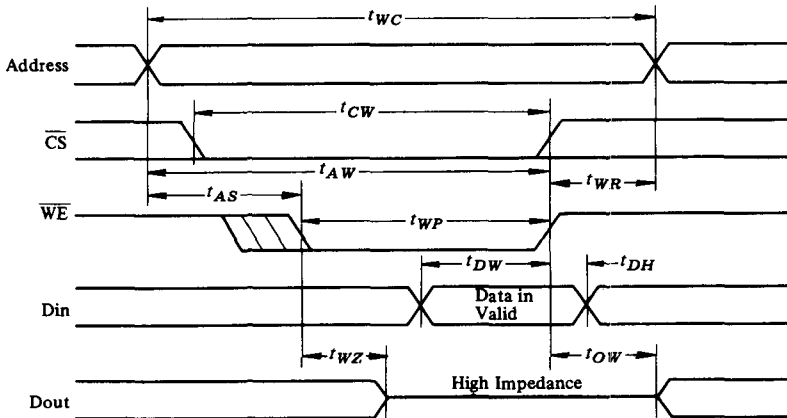


● WRITE CYCLE

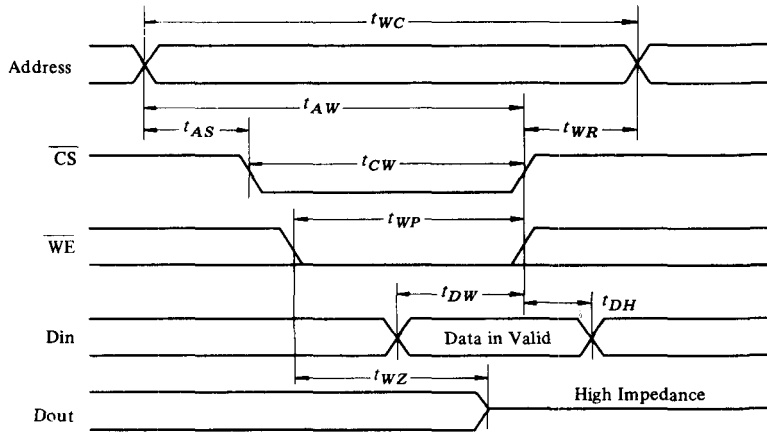
Item	Symbol	HM6167HLP-45		HM6167HLP-55		Unit	Notes
		min	max	min	max		
Write Cycle Time	t_{WC}	45	-	55	-	ns	(2)
Chip Selection to End of Write	t_{CW}	40	-	50	-	ns	
Address Valid to End of Write	t_{AW}	40	-	50	-	ns	
Address Setup Time	t_{AS}	0	-	0	-	ns	
Write Pulse Width	t_{WP}	25	-	35	-	ns	
Write Recovery Time	t_{WR}	0	-	0	-	ns	
Data Valid to End of Write	t_{DW}	25	-	25	-	ns	
Data Hold Time	t_{DH}	0	-	0	-	ns	
Write Enable to Output in High Z	t_{WZ}	0	25	0	25	ns	(3) (4)
Output Active from End of Write	t_{OW}	0	-	0	-	ns	(3) (4)

- NOTES: 1. If \overline{CS} goes high simultaneously with \overline{WE} high, the output remains in a high impedance states.
 2. All Write Cycle timings are referenced from the last valid address to the first transitions address.
 3. Transition is measured $\pm 500\text{mV}$ from steady state voltage with specified loading in Load B.
 4. This parameter is sampled and not 100% tested.

● TIMING WAVEFORM OF WRITE CYCLE NO. 1 (\overline{WE} Controlled)



● TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{\text{CS}}$ Controlled)



■ LOW V_{CC} DATA RETENTION CHARACTERISTICS ($T_a=0^\circ\text{C}$ to 70°C)

Parameter	Symbol	Test Condition	min	typ	max	Unit
V_{CC} for Data Retention	V_{DR}		2.0	—	—	V
Data Retention Current	I_{CCDR}	$\overline{\text{CS}} \geq V_{CC} - 0.2\text{V}$ $V_{in} \geq V_{CC} - 0.2\text{V}$ or $0\text{V} \leq V_{in} \leq 0.2\text{V}$	—	—	20*	μA
Chip Deselect to Data Retention Time	t_{CDR}		0	—	—	ns
Operation Recovery Time	t_R		t_{RC}^Δ	—	—	ns

Δt_{RC} - Read Cycle Time

* $V_{CC} = 2.0\text{V}$
** $V_{CC} = 3.0\text{V}$

● LOW V_{CC} DATA RETENTION WAVEFORM

