

4-Mbit (256K x 16) Static RAM

Features

- Very high speed: 45 ns
- Temperature ranges
 - Industrial: -40 °C to +85 °C
- Wide voltage range: 2.20 V to 3.60 V
- Pin compatible with CY62147DV30
- Ultra low standby power
 - Typical standby current: 1 μ A
 - Maximum standby current: 7 μ A (Industrial)
- Ultra low active power
 - Typical active current: 2 mA at f = 1 MHz
- Easy memory expansion with \overline{CE} [1] and \overline{OE} features
- Automatic power-down when deselected
- Complementary metal oxide semiconductor (CMOS) for optimum speed and power
- Available in Pb-free 48-ball very fine ball grid array (VFBGA) (single/dual CE option) and 44-pin thin small outline package (TSOP) II packages
- Byte power-down feature

Functional Description

The CY62147EV30 is a high performance CMOS static RAM (SRAM) organized as 256K words by 16 bits. This device features advanced circuit design to provide ultra low active current. It is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device

also has an automatic power down feature that significantly reduces power consumption when addresses are not toggling. Placing the device into standby mode reduces power consumption by more than 99 percent when deselected (\overline{CE} HIGH or both \overline{BLE} and \overline{BHE} are HIGH). The input and output pins (I/O_0 through I/O_{15}) are placed in a high impedance state when:

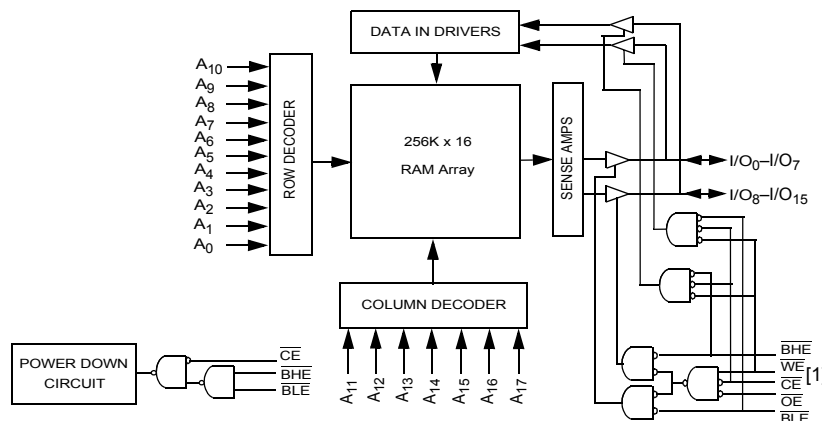
- Deselected (\overline{CE} HIGH)
- Outputs are disabled (\overline{OE} HIGH)
- Both Byte High Enable and Byte Low Enable are disabled (\overline{BHE} , \overline{BLE} HIGH)
- Write operation is active (\overline{CE} LOW and \overline{WE} LOW)

To write to the device, take Chip Enable (\overline{CE}) and Write Enable (\overline{WE}) inputs LOW. If Byte Low Enable (\overline{BLE}) is LOW, then data from I/O pins (I/O_0 through I/O_7) is written into the location specified on the address pins (A_0 through A_{17}). If Byte High Enable (\overline{BHE}) is LOW, then data from I/O pins (I/O_8 through I/O_{15}) is written into the location specified on the address pins (A_0 through A_{17}).

To read from the device, take Chip Enable (\overline{CE}) and Output Enable (\overline{OE}) LOW while forcing the Write Enable (\overline{WE}) HIGH. If Byte Low Enable (\overline{BLE}) is LOW, then data from the memory location specified by the address pins appear on I/O_0 to I/O_7 . If Byte High Enable (\overline{BHE}) is LOW, then data from memory appears on I/O_8 to I/O_{15} . See the Truth Table on page 10 for a complete description of read and write modes.

For best practice recommendations, refer to the Cypress application note AN1064, SRAM System Guidelines.

Logic Block Diagram



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Note

1. BGA packaged device is offered in single CE and dual CE options. In this data sheet, for a dual CE device, \overline{CE} refers to the internal logical combination of \overline{CE}_1 and \overline{CE}_2 such that when \overline{CE}_1 is LOW and \overline{CE}_2 is HIGH, \overline{CE} is LOW. For all other cases \overline{CE} is HIGH.

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Product Portfolio

| Product | Range | V _{CC} Range (V) | | | Speed (ns) | Power Dissipation | | | | | |
|---------------|--------------------|---------------------------|--------------------|-----|--------------------|--------------------------------|--------------------|----------------------|----|-------------------------------|---|
| | | | | | | Operating I _{CC} (mA) | | | | Standby I _{SB2} (μA) | |
| | | | | | | f = 1 MHz | | f = f _{max} | | | |
| Min | Typ ^[2] | Max | Typ ^[2] | Max | Typ ^[2] | Max | Typ ^[2] | Max | | | |
| CY62147EV30LL | Industrial | 2.2 | 3.0 | 3.6 | 45 ns | 2 | 2.5 | 15 | 20 | 1 | 7 |

Pin Configuration

Figure 1. 48-Ball VFBGA (Single Chip Enable)^[3, 4]

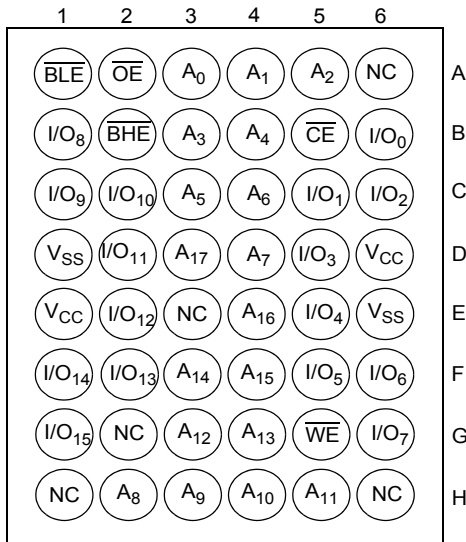


Figure 2. 48-Ball VFBGA (Dual Chip Enable)^[3, 4]

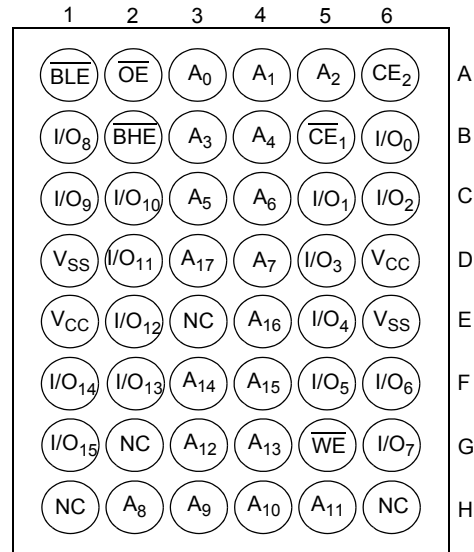
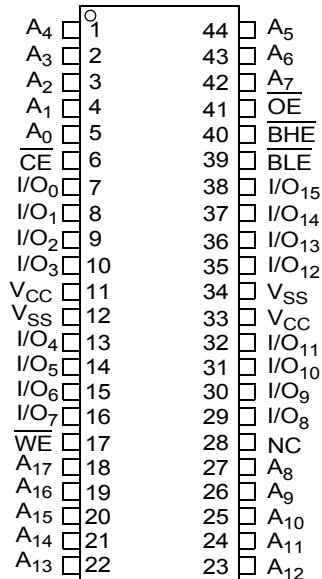


Figure 3. 44-Pin TSOP II^[3]



Notes

- 2. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC(typ)}, T_A = 25 °C.
- 3. NC pins are not connected on the die.
- 4. Pins H1, G2, and H6 in the BGA package are address expansion pins for 8 Mb, 16 Mb, and 32 Mb, respectively.

Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. User guidelines are not tested.

Storage temperature -65 °C to + 150 °C

Ambient temperature with power applied -55 °C to + 125 °C

Supply voltage to ground potential -0.3 V to + 3.9 V ($V_{CCmax} + 0.3$ V)

DC voltage applied to outputs in High Z state ^[5, 6] -0.3 V to 3.9 V ($V_{CCmax} + 0.3$ V)

DC input voltage ^[5, 6] -0.3 V to 3.9 V ($V_{CCmax} + 0.3$ V)

Output current into outputs (LOW) 20 mA

Static discharge voltage >2001 V (MIL-STD-883, method 3015)

Latch-up current >200 mA

Operating Range

| Device | Range | Ambient Temperature | V_{CC} ^[7] |
|---------------|------------|---------------------|-------------------------|
| CY62147EV30LL | Industrial | -40 °C to +85 °C | 2.2 V to 3.6 V |

Electrical Characteristics

Over the Operating Range

| Parameter | Description | Test Conditions | 45 ns (Industrial) | | | Unit |
|---------------------------------|---|--|--------------------|--------------------|-----------------------|------|
| | | | Min | Typ ^[8] | Max | |
| V _{OH} | Output HIGH voltage | I _{OH} = -0.1 mA | 2.0 | - | - | V |
| | | I _{OH} = -1.0 mA, V _{CC} ≥ 2.70 V | 2.4 | - | - | V |
| V _{OL} | Output LOW voltage | I _{OL} = 0.1 mA | - | - | 0.4 | V |
| | | I _{OL} = 2.1 mA, V _{CC} = 2.70 V | - | - | 0.4 | V |
| V _{IH} | Input HIGH voltage | V _{CC} = 2.2 V to 2.7 V | 1.8 | - | V _{CC} + 0.3 | V |
| | | V _{CC} = 2.7 V to 3.6 V | 2.2 | - | V _{CC} + 0.3 | V |
| V _{IL} | Input LOW voltage | V _{CC} = 2.2 V to 2.7 V | -0.3 | - | 0.6 | V |
| | | V _{CC} = 2.7 V to 3.6 V | -0.3 | - | 0.8 | V |
| I _{IX} | Input leakage current | GND ≤ V _I ≤ V _{CC} | -1 | - | +1 | μA |
| I _{OZ} | Output leakage current | GND ≤ V _O ≤ V _{CC} , output disabled | -1 | - | +1 | μA |
| I _{CC} | V _{CC} operating supply current | f = f _{max} = 1/t _{RC} f = 1 MHz | - | 15 | 20 | mA |
| | | V _{CC} = V _{CC(max)} I _{OUT} = 0 mA CMOS levels | - | 2 | 2.5 | |
| I _{SB1} | Automatic CE power-down current—CMOS inputs | $\overline{CE} \geq V_{CC} - 0.2$ V V _{IN} ≥ V _{CC} - 0.2 V, V _{IN} ≤ 0.2 V f = f _{max} (address and data only), f = 0 (OE, BHE, BLE and WE), V _{CC} = 3.60 V | - | 1 | 7 | μA |
| I _{SB2} ^[9] | Automatic CE power-down current—CMOS inputs | $\overline{CE} \geq V_{CC} - 0.2$ V V _{IN} ≥ V _{CC} - 0.2 V or V _{IN} ≤ 0.2 V, f = 0, V _{CC} = 3.60 V | - | 1 | 7 | μA |

Capacitance

For all packages. ^[10]

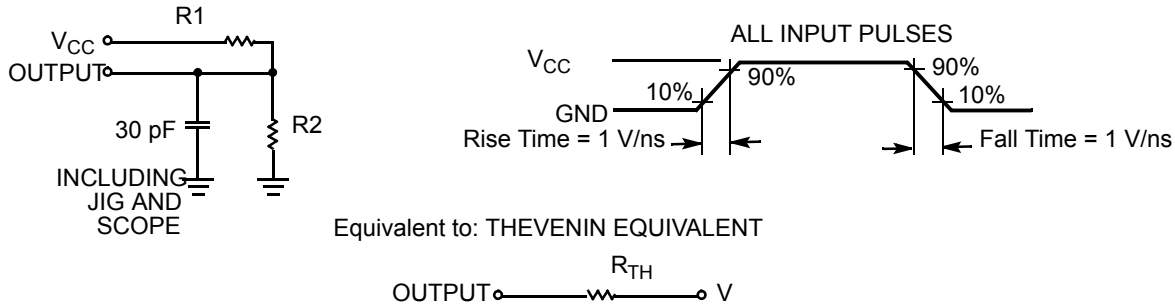
| Parameter | Description | Test Conditions | Max | Unit |
|------------------|--------------------|--|-----|------|
| C _{IN} | Input capacitance | T _A = 25 °C, f = 1 MHz, | 10 | pF |
| C _{OUT} | Output capacitance | V _{CC} = V _{CC(typ)} | 10 | pF |

Notes

- V_{IL(min)} = -2.0 V for pulse durations less than 20 ns.
- V_{IH(max)} = V_{CC} + 0.75 V for pulse durations less than 20 ns.
- Full device AC operation assumes a minimum of 100 μs ramp time from 0 to V_{CC(min)} and 200 μs wait time after V_{CC} stabilization.
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC(typ)}, T_A = 25 °C.
- Chip enable (CE) and byte enables (BHE and BLE) need to be tied to CMOS levels to meet the I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.
- Tested initially and after any design or process changes that may affect these parameters.

Thermal Resistance^[11]

| Parameter | Description | Test Conditions | VFBGA Package | TSOP II Package | Unit |
|---------------|--|--|---------------|-----------------|--------|
| Θ_{JA} | Thermal resistance (junction to ambient) | Still Air, soldered on a 3 × 4.5 inch, two-layer printed circuit board | 75 | 77 | °C / W |
| Θ_{JC} | Thermal resistance (junction to case) | | 10 | 13 | °C / W |

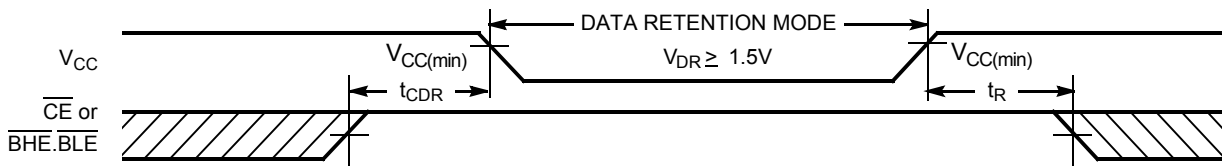
Figure 4. AC Test Load and Waveforms


| Parameters | 2.50 V | 3.0 V | Unit |
|------------|--------|-------|----------|
| R1 | 16667 | 1103 | Ω |
| R2 | 15385 | 1554 | Ω |
| R_{TH} | 8000 | 645 | Ω |
| V_{TH} | 1.20 | 1.75 | V |

Data Retention Characteristics

Over the Operating Range

| Parameter | Description | Conditions | Min | Typ ^[12] | Max | Unit |
|-------------------|--------------------------------------|---|-----|---------------------|-----|---------------|
| V_{DR} | V_{CC} for data retention | | 1.5 | – | – | V |
| $I_{CCDR}^{[13]}$ | Data retention current | $V_{CC} = 1.5\text{ V}$, $\overline{CE} \geq V_{CC} - 0.2\text{ V}$, $V_{IN} \geq V_{CC} - 0.2\text{ V}$ or $V_{IN} \leq 0.2\text{ V}$ | – | 0.8 | 7 | μA |
| $t_{CDR}^{[11]}$ | Chip deselect to data retention time | | 0 | – | – | ns |
| $t_R^{[14]}$ | Operation recovery time | | 45 | – | – | ns |

Figure 5. Data Retention Waveform^[15, 16]

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Notes

- Tested initially and after any design or process changes that may affect these parameters
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, $T_A = 25^\circ\text{C}$.
- Chip enable (\overline{CE}) and byte enables (\overline{BHE} and \overline{BLE}) need to be tied to CMOS levels to meet the I_{SB2} / I_{CCDR} spec. Other inputs can be left floating..
- Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)} \geq 100\ \mu\text{s}$ or stable at $V_{CC(min)} \geq 100\ \mu\text{s}$.
- BGA packaged device is offered in single CE and dual CE options. In this data sheet, for a dual CE device, \overline{CE} refers to the internal logical combination of \overline{CE}_1 and \overline{CE}_2 , such that when \overline{CE}_1 is LOW and \overline{CE}_2 is HIGH, \overline{CE} is LOW. For all other cases \overline{CE} is HIGH.
- $\overline{BHE.BLE}$ is the AND of both \overline{BHE} and \overline{BLE} . Deselect the chip by either disabling the chip enable signals or by disabling both \overline{BHE} and \overline{BLE} .

Switching Characteristics

Over the Operating Range [17, 18]

| Parameter | Description | 45 ns (Industrial) | | Unit |
|-----------------------------------|--|--------------------|-----|------|
| | | Min | Max | |
| Read Cycle | | | | |
| t_{RC} | Read cycle time | 45 | – | ns |
| t_{AA} | Address to data valid | – | 45 | ns |
| t_{OHA} | Data hold from address change | 10 | – | ns |
| t_{ACE} | \overline{CE} LOW to data valid | – | 45 | ns |
| t_{DOE} | \overline{OE} LOW to data valid | – | 22 | ns |
| t_{LZOE} | \overline{OE} LOW to LOW Z ^[19] | 5 | – | ns |
| t_{HZOE} | \overline{OE} HIGH to High Z ^[19, 20] | – | 18 | ns |
| t_{LZCE} | \overline{CE} LOW to Low Z ^[19] | 10 | – | ns |
| t_{HZCE} | \overline{CE} HIGH to High Z ^[19, 20] | – | 18 | ns |
| t_{PU} | \overline{CE} LOW to power-up | 0 | – | ns |
| t_{PD} | \overline{CE} HIGH to power-down | – | 45 | ns |
| t_{DBE} | $\overline{BLE}/\overline{BHE}$ LOW to data valid | – | 45 | ns |
| t_{LZBE} | $\overline{BLE}/\overline{BHE}$ LOW to Low Z ^[19] | 10 | – | ns |
| t_{HZBE} | $\overline{BLE}/\overline{BHE}$ HIGH to HIGH Z ^[19, 20] | – | 18 | ns |
| Write Cycle^[21] | | | | |
| t_{WC} | Write cycle time | 45 | – | ns |
| t_{SCE} | \overline{CE} LOW to write end | 35 | – | ns |
| t_{AW} | Address setup to write end | 35 | – | ns |
| t_{HA} | Address hold from write end | 0 | – | ns |
| t_{SA} | Address setup to write start | 0 | – | ns |
| t_{PWE} | \overline{WE} pulse width | 35 | – | ns |
| t_{BW} | $\overline{BLE}/\overline{BHE}$ LOW to write end | 35 | – | ns |
| t_{SD} | Data setup to write end | 25 | – | ns |
| t_{HD} | Data hold from write end | 0 | – | ns |
| t_{HZWE} | \overline{WE} LOW to High Z ^[19, 20] | – | 18 | ns |
| t_{LZWE} | \overline{WE} HIGH to Low Z ^[19] | 10 | – | ns |

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Notes

17. Test conditions for all parameters other than tri-state parameters assume signal transition time of 3 ns (1V/ns) or less, timing reference levels of $V_{CC(typ)}/2$, input pulse levels of 0 to $V_{CC(typ)}$, and output loading of the specified I_{OL}/I_{OH} as shown in the [AC Test Load and Waveforms on page 5](#).
18. AC timing parameters are subject to byte enable signals (BHE or BLE) not switching when chip is disabled. See application note [AN13842](#) for further clarification.
19. At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZBE} is less than t_{LZBE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any device.
20. t_{HZOE} , t_{HZCE} , t_{HZBE} , and t_{HZWE} transitions are measured when the outputs enter a high impedance state.
21. The internal write time of the memory is defined by the overlap of \overline{WE} , $\overline{CE} = V_{IL}$, \overline{BHE} , \overline{BLE} , or both = V_{IL} . All signals must be active to initiate a write and any of these signals can terminate a write by going inactive. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.

Switching Waveforms

Figure 6. Read Cycle No. 1: Address Transition Controlled^[22, 23]

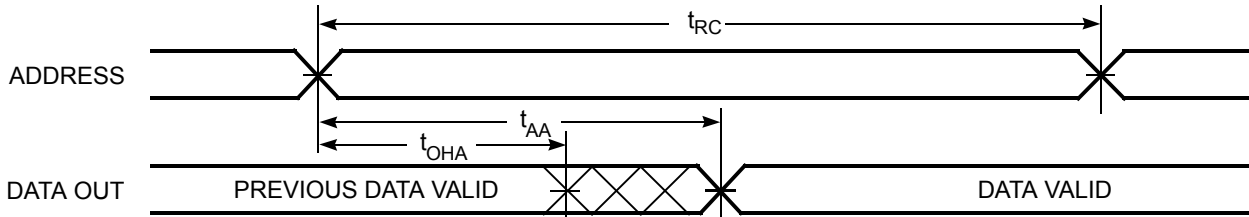
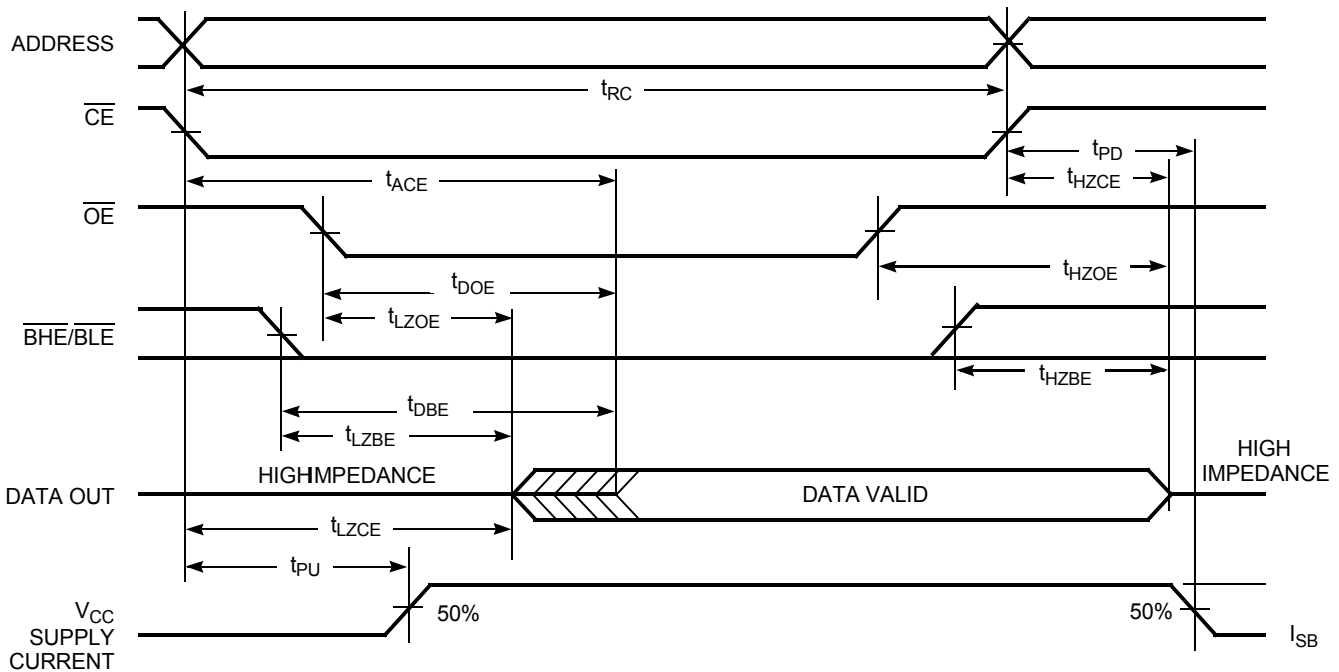


Figure 7. Read Cycle No. 2: \overline{OE} Controlled^[23, 24, 25]



Notes

22. The device is continuously selected. \overline{OE} , $\overline{CE} = V_{IL}$, \overline{BHE} , \overline{BLE} , or both = V_{IL} .

23. \overline{WE} is HIGH for read cycle.

24. BGA packaged device is offered in single CE and dual CE options. In this data sheet, for a dual CE device, \overline{CE} refers to the internal logical combination of \overline{CE}_1 and \overline{CE}_2 such that when \overline{CE}_1 is LOW and \overline{CE}_2 is HIGH, \overline{CE} is LOW. For all other cases \overline{CE} is HIGH.

25. Address valid before or similar to \overline{CE} and \overline{BHE} , \overline{BLE} transition LOW.

Switching Waveforms (continued)

Figure 8. Write Cycle No. 1: $\overline{\text{WE}}$ Controlled^[26, 27, 28, 29]

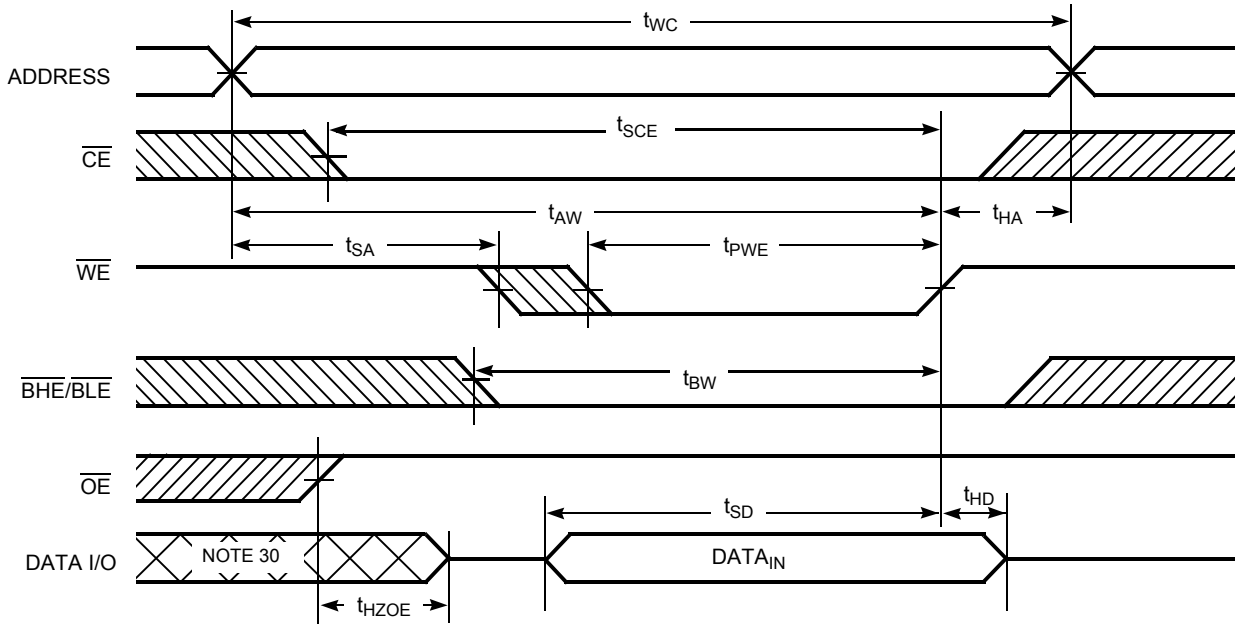
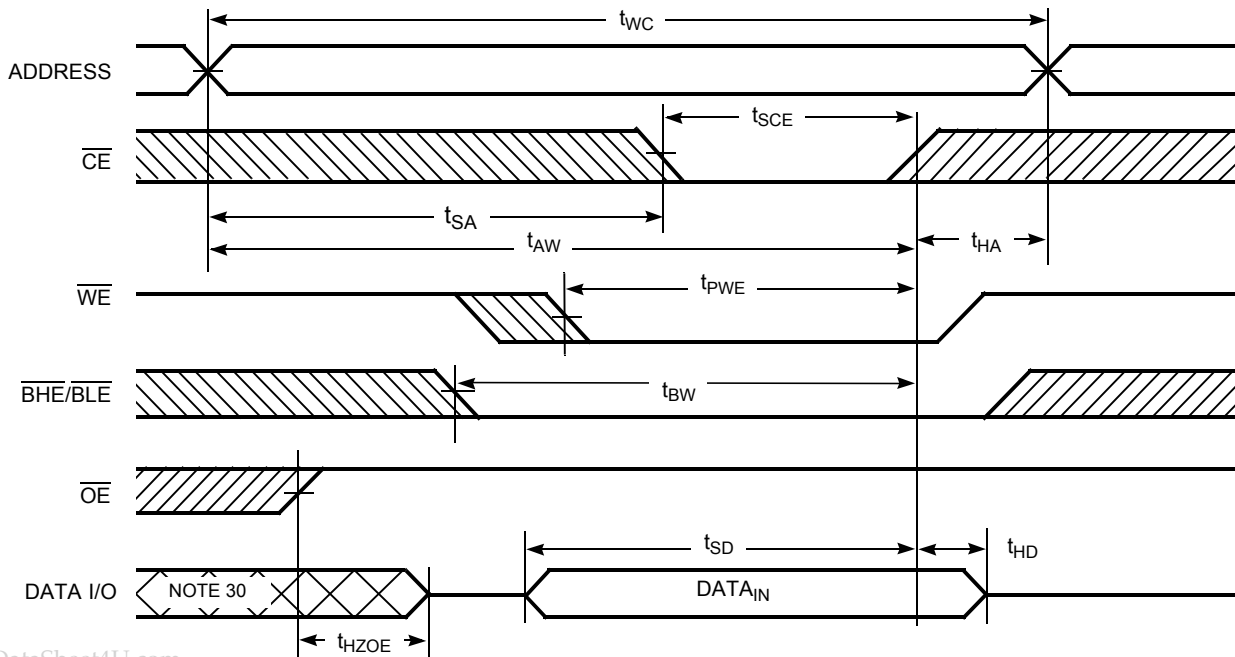


Figure 9. Write Cycle No. 2: $\overline{\text{CE}}$ Controlled^[26, 27, 28, 29]



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Notes

- 26. BGA packaged device is offered in single CE and dual CE options. In this data sheet, for a dual CE device, $\overline{\text{CE}}$ refers to the internal logical combination of $\overline{\text{CE}}_1$ and CE_2 such that when CE_1 is LOW and CE_2 is HIGH, $\overline{\text{CE}}$ is LOW. For all other cases $\overline{\text{CE}}$ is HIGH.
- 27. The internal write time of the memory is defined by the overlap of $\overline{\text{WE}}$, $\overline{\text{CE}} = V_{\text{IL}}$, $\overline{\text{BHE}}$, $\overline{\text{BLE}}$, or both = V_{IL} . All signals must be active to initiate a write and any of these signals can terminate a write by going inactive. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.
- 28. Data I/O is high impedance if $\text{OE} = V_{\text{IH}}$.
- 29. If $\overline{\text{CE}}$ goes HIGH simultaneously with $\overline{\text{WE}} = V_{\text{IH}}$, the output remains in a high impedance state.
- 30. During this period, the I/Os are in output state. Do not apply input signals.

Switching Waveforms (continued)

Figure 10. Write Cycle No. 3: \overline{WE} Controlled, \overline{OE} LOW^[31, 32]

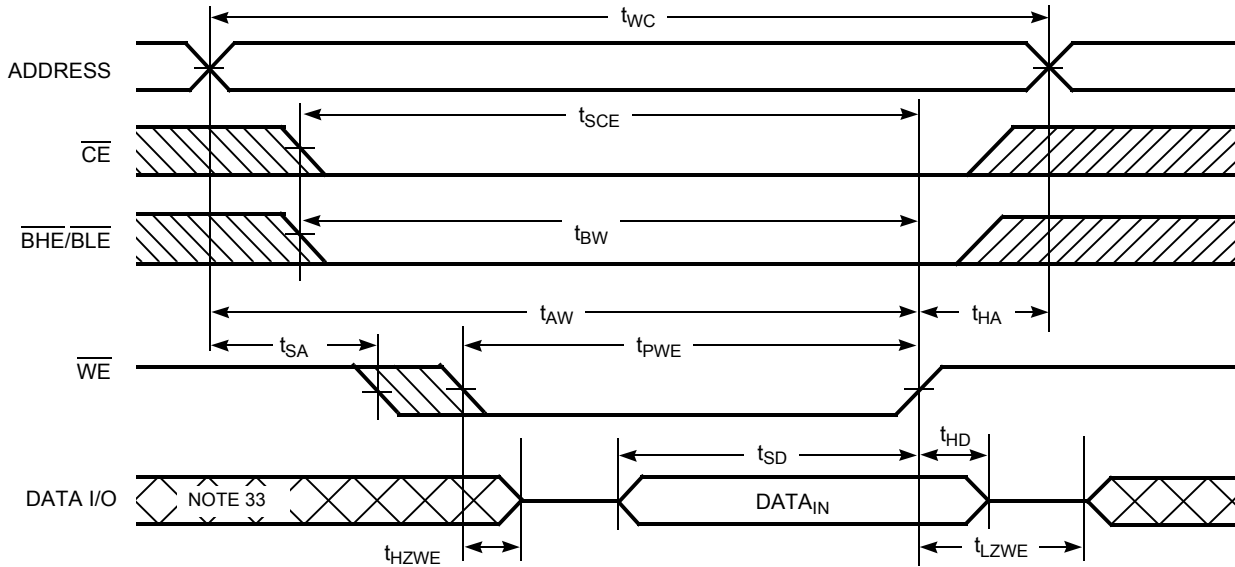
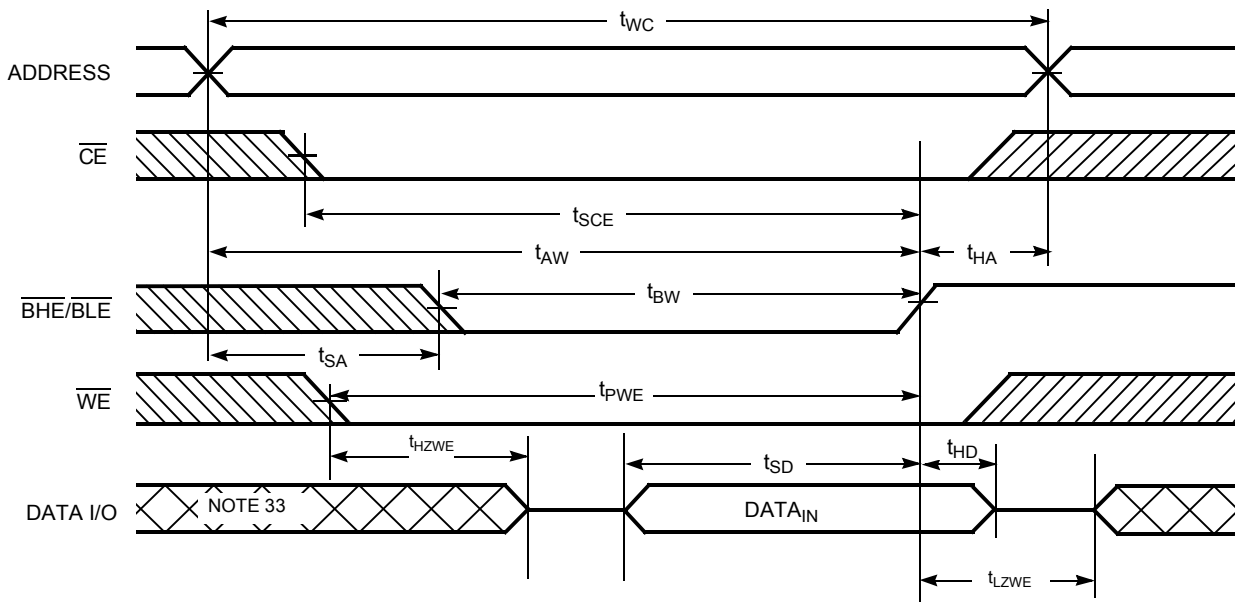


Figure 11. Write Cycle No. 4: $\overline{BHE}/\overline{BLE}$ Controlled, \overline{OE} LOW^[31, 32]



Notes

- 31. BGA packaged device is offered in single CE and dual CE options. In this data sheet, for a dual CE device, \overline{CE} refers to the internal logical combination of \overline{CE}_1 and \overline{CE}_2 such that when \overline{CE}_1 is LOW and \overline{CE}_2 is HIGH, \overline{CE} is LOW. For all other cases \overline{CE} is HIGH.
- 32. If \overline{CE} goes HIGH simultaneously with $WE = V_{IH}$, the output remains in a high impedance state.
- 33. During this period, the I/Os are in output state. Do not apply input signals.

Truth Table

| \overline{CE} ^[34, 35] | \overline{WE} | \overline{OE} | \overline{BHE} | \overline{BLE} | I/Os | Mode | Power |
|-------------------------------------|-----------------|-----------------|------------------|------------------|--|---------------------|----------------------|
| H | X | X | X | X | High Z | Deselect/Power-down | Standby (I_{SB}) |
| L | X | X | H | H | High Z | Deselect/Power-down | Standby (I_{SB}) |
| L | H | L | L | L | Data out (I/O ₀ –I/O ₁₅) | Read | Active (I_{CC}) |
| L | H | L | H | L | Data out (I/O ₀ –I/O ₇); I/O ₈ –I/O ₁₅ in High Z | Read | Active (I_{CC}) |
| L | H | L | L | H | Data out (I/O ₈ –I/O ₁₅); I/O ₀ –I/O ₇ in High Z | Read | Active (I_{CC}) |
| L | H | H | L | L | High Z | Output disabled | Active (I_{CC}) |
| L | H | H | H | L | High Z | Output disabled | Active (I_{CC}) |
| L | H | H | L | H | High Z | Output disabled | Active (I_{CC}) |
| L | L | X | L | L | Data in (I/O ₀ –I/O ₁₅) | Write | Active (I_{CC}) |
| L | L | X | H | L | Data in (I/O ₀ –I/O ₇); I/O ₈ –I/O ₁₅ in High Z | Write | Active (I_{CC}) |
| L | L | X | L | H | Data in (I/O ₈ –I/O ₁₅); I/O ₀ –I/O ₇ in High Z | Write | Active (I_{CC}) |

Notes

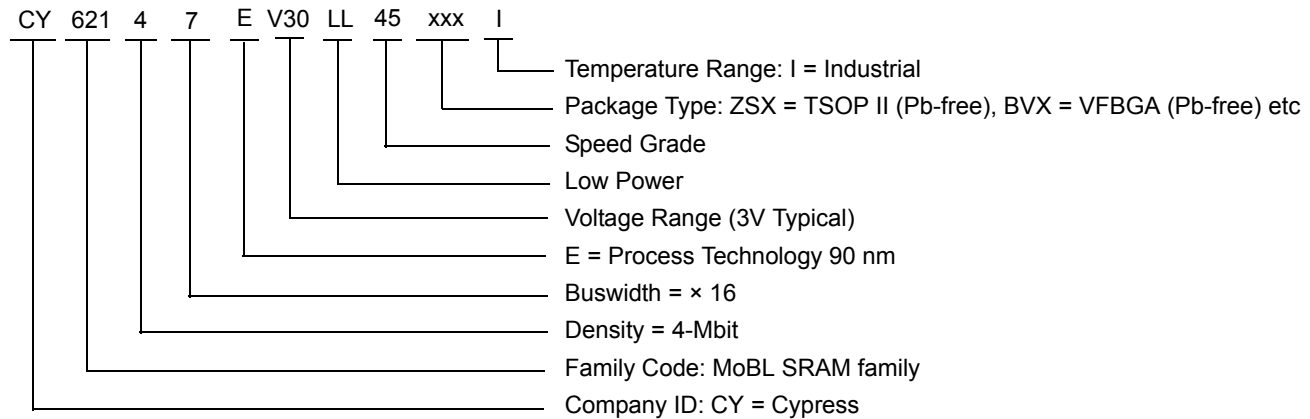
34. BGA packaged device is offered in single CE and dual CE options. In this data sheet, for a dual CE device, \overline{CE} refers to the internal logical combination of \overline{CE}_1 and \overline{CE}_2 such that when \overline{CE}_1 is LOW and \overline{CE}_2 is HIGH, \overline{CE} is LOW. For all other cases \overline{CE} is HIGH.
35. For the Dual Chip Enable device, \overline{CE} refers to the internal logical combination of \overline{CE}_1 and \overline{CE}_2 such that when \overline{CE}_1 is LOW and \overline{CE}_2 is HIGH, \overline{CE} is LOW. For all other cases \overline{CE} is HIGH. Intermediate voltage levels is not permitted on any of the Chip Enable pins (CE for the Single Chip Enable device; \overline{CE}_1 and \overline{CE}_2 for the Dual Chip Enable device).

Ordering Information

| Speed (ns) | Ordering Code | Package Diagram | Package Type | Operating Range |
|------------|----------------------|-----------------|---|-----------------|
| 45 | CY62147EV30LL-45BVI | 51-85150 | 48-Ball Very Fine Pitch Ball Grid Array ^[36] | Industrial |
| | CY62147EV30LL-45BVXI | 51-85150 | 48-Ball Very Fine Pitch Ball Grid Array (Pb-free) ^[36] | |
| | CY62147EV30LL-45B2XI | 51-85150 | 48-Ball Very Fine Pitch Ball Grid Array (Pb-free) ^[37] | |
| | CY62147EV30LL-45ZSXI | 51-85087 | 44-Pin Thin Small Outline Package II (Pb-free) | |

Contact your local Cypress sales representative for availability of these parts.

Ordering Code Definitions

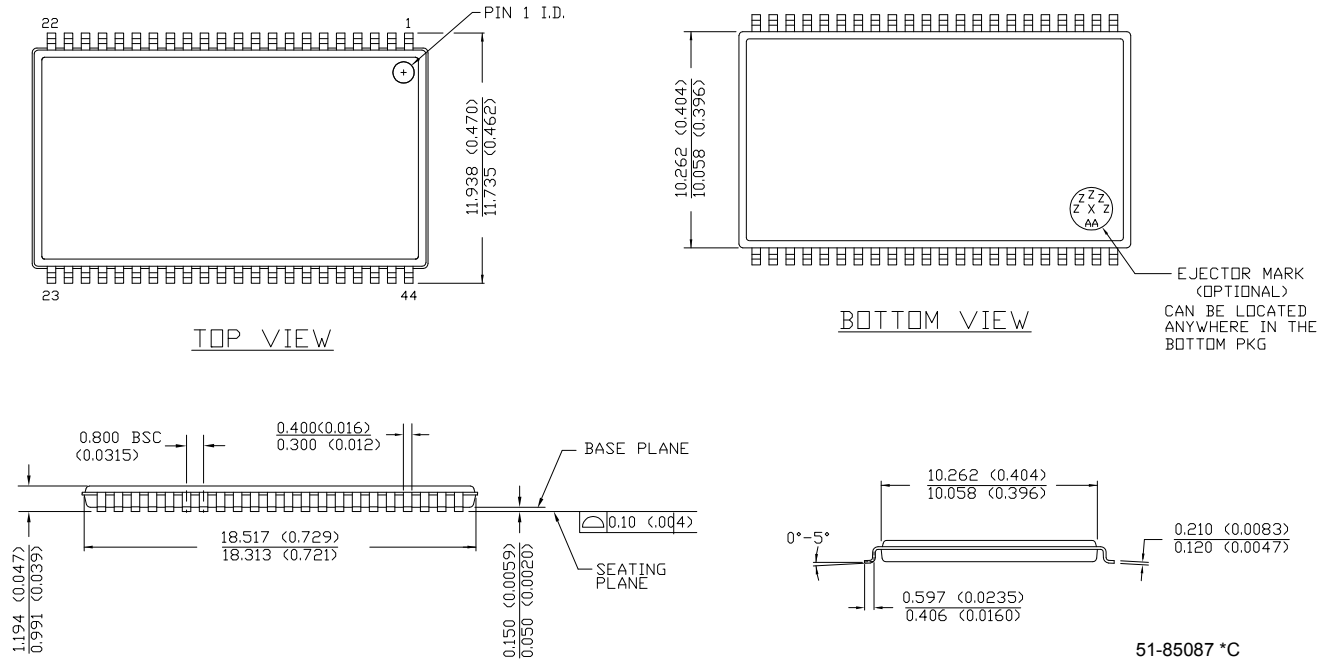


Notes

- 36. This BGA package is offered with single chip enable.
- 37. This BGA package is offered with dual chip enable.

Package Diagrams (continued)

Figure 13. 44-Pin TSOP II, 51-85087



Acronyms

| Acronym | Description |
|---------|---|
| CMOS | complementary metal oxide semiconductor |
| I/O | input/output |
| SRAM | static random access memory |
| VFBGA | very fine ball grid array |
| TSOP | thin small outline package |

Document Conventions

Units of Measure

| Symbol | Unit of Measure |
|--------|-----------------|
| °C | degrees Celsius |
| μA | microamperes |
| mA | milliamperes |
| MHz | megahertz |
| ns | nanoseconds |
| pF | picofarads |
| V | volts |
| Ω | ohms |
| W | watts |

Document History Page

| Document Title: CY62147EV30 MoBL® 4-Mbit (256K x 16) Static RAM Document Number: 38-05440 | | | | |
|--|---------|-----------------|-----------------|--|
| Rev. | ECN No. | Orig. of Change | Submission Date | Description of Change |
| ** | 201861 | AJU | 01/13/04 | New Data Sheet |
| *A | 247009 | SYT | See ECN | <p>Changed from Advanced Information to Preliminary</p> <p>Moved Product Portfolio to Page 2</p> <p>Changed Vcc stabilization time in footnote #8 from 100 μs to 200 μs</p> <p>Removed Footnote #15(t_{LZBE}) from Previous Revision</p> <p>Changed I_{CCDR} from 2.0 μA to 2.5 μA</p> <p>Changed typo in Data Retention Characteristics(t_R) from 100 μs to t_{RC} ns</p> <p>Changed t_{OHA} from 6 ns to 10 ns for both 35 ns and 45 ns Speed Bin</p> <p>Changed t_{HZOE}, t_{HZBE}, t_{HZWE} from 12 to 15 ns for 35 ns Speed Bin and 15 to 18 ns for 45 ns Speed Bin</p> <p>Changed t_{SCE} and t_{BW} from 25 to 30 ns for 35 ns Speed Bin and 40 to 35 ns for 45 ns Speed Bin</p> <p>Changed t_{HZCE} from 12 to 18 ns for 35 ns Speed Bin and 15 to 22 ns for 45 ns Speed Bin</p> <p>Changed t_{SD} from 15 to 18 ns for 35 ns Speed Bin and 20 to 22 ns for 45 ns Speed Bin</p> <p>Changed t_{DOE} from 15 to 18 ns for 35 ns Speed Bin</p> <p>Changed Ordering Information to include Pb-Free Packages</p> |
| *B | 414807 | ZSD | See ECN | <p>Changed from Preliminary information to Final</p> <p>Changed the address of Cypress Semiconductor Corporation on Page #1 from "3901 North First Street" to "198 Champion Court"</p> <p>Removed 35ns Speed Bin, "L" version of CY62147EV30</p> <p>Changed ball E3 from DNU to NC.</p> <p>Removed redundant foot note on DNU.</p> <p>Changed I_{CC} (Max) value from 2 mA to 2.5 mA and I_{CC} (Typ) value from 1.5 mA to 2 mA at $f=1$ MHz</p> <p>Changed I_{CC} (Typ) value from 12 mA to 15 mA at $f = f_{max}$</p> <p>Changed I_{SB1} and I_{SB2} Typ values from 0.7 μA to 1 μA and Max values from 2.5 μA to 7 μA.</p> <p>Changed I_{CCDR} from 2.5 μA to 7 μA.</p> <p>Added I_{CCDR} typical value.</p> <p>Changed AC test load capacitance from 50 pF to 30 pF on Page #4, changed t_{LZOE} from 3 ns to 5 ns, changed t_{LZCE}, t_{LZBE} and t_{LZWE} from 6 ns to 10 ns, changed t_{HZCE} from 22 ns to 18 ns, changed t_{PWE} from 30 ns to 35 ns and changed t_{SD} from 22 ns to 25 ns.</p> <p>Updated the package diagram 48-pin VFBGA from *B to *D</p> <p>Updated the ordering information table and replaced the Package Name column with Package Diagram.</p> |
| *C | 464503 | NXR | See ECN | <p>Included Automotive Range in product offering</p> <p>Updated the Ordering Information</p> |
| *D | 925501 | VKN | See ECN | <p>Added Preliminary Automotive-A information</p> <p>Added footnote #9 related to I_{SB2} and I_{CCDR}</p> <p>Added footnote #14 related AC timing parameters</p> |
| *E | 1045701 | VKN | See ECN | <p>Converted Automotive-A and Automotive -E specs from preliminary to final</p> |
| *F | 2577505 | VKN/PYRS | 10/03/08 | <p>Added -45B2XI part (Dual CE option)</p> |
| *G | 2681901 | VKN/PYRS | 04/01/09 | <p>Added CY62147EV30LL-45ZSXA in the ordering information table</p> |
| *H | 2886488 | AJU | 03/02/2010 | <p>Updated package diagrams.</p> <p>Added Contents.</p> <p>Updated links in Sales, Solutions, and Legal Information.</p> <p>Added Note 23.</p> |
| *I | 3109050 | 12/13/2010 | PRAS | <p>Changed Table Footnotes to Footnotes.</p> <p>Added Ordering Code Definitions.</p> |

Document Title: CY62147EV30 MoBL[®] 4-Mbit (256K x 16) Static RAM
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| Rev. | ECN No. | Orig. of Change | Submission Date | Description of Change |
|------|---------|-----------------|-----------------|---|
| *J | 3123973 | RAME | 01/31/2011 | Separated Industrial and Auto parts from this datasheet Removed Automotive info Added Acronyms and Units of Measure table |

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