

# TLP552

Isolated Line Receiver  
 Simplex/Multiplex Data Transmission  
 Computer-Peripheral Interface  
 Microprocessor System Interface  
 Digital Isolation for A-D, D-A Conversion

The TOSHIBA TLP552 is a photocoupler which combines a GaAlAs IRED LED as the emitter and an integrated high gain, high speed photodetector. This unit is 8-lead DIP.

The output of the detector circuit is an open collector, schottky clamped transistor.

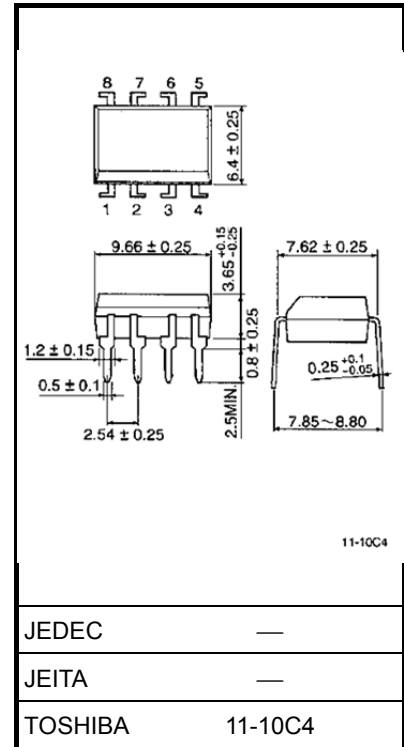
- TTL/LSTTL compatible:  $V_{CC} = 5\text{ V}$
- Isolation voltage:  $2500\text{ V}_{\text{RMS}}$  (min)
- Switching speed:  $t_{\text{pHL}}, t_{\text{pLH}} = 60\text{ ns}$  (typ.) ( $@R_L = 350\ \Omega$ )
- Guaranteed performance over temp.:  $0\text{ to }70^\circ\text{C}$
- UL recognized: UL1577, file no. E67349

### Truth Table (positive logic)

Input	Enable	Output
H	H	L
L	H	H
H	L	H
L	L	H

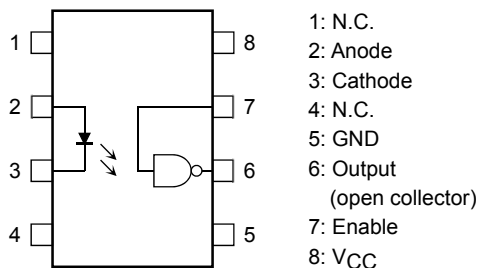
Note: A  $0.1\ \mu\text{F}$  bypass capacitor must be connected between pins 8 and 5 (see "Instruction for use" on page 3).

Unit: mm

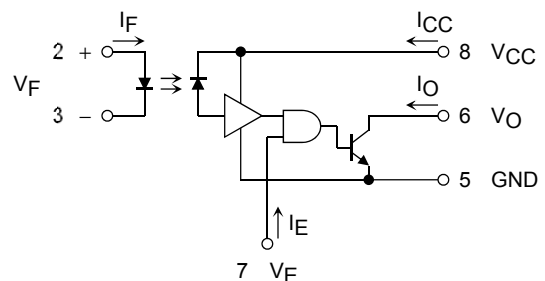


Weight: 0.54 g (typ.)

### Pin Configurations (top view)



### Schematic



Start of commercial production  
 1982/08

## Absolute Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit
LED	Forward current	I <sub>F</sub>	20	mA
	Pulse forward current (Note 1)	I <sub>FP</sub>	40	mA
	Peak transient forward current (Note 2)	I <sub>FPT</sub>	0.5	A
	Reverse voltage	V <sub>R</sub>	5	V
	Diode power dissipation	P <sub>D</sub>	40	mW
Detector	Output current	I <sub>O</sub>	50	mA
	Output voltage	V <sub>O</sub>	7	V
	Supply voltage (Note 3)	V <sub>CC</sub>	7	V
	Enable input voltage (Note 4)	V <sub>E</sub>	5.5	V
	Output collector power dissipation	P <sub>O</sub>	85	mW
Operating temperature range		T <sub>opr</sub>	0 to 70	°C
Storage temperature range		T <sub>stg</sub>	-55 to 125	°C
Lead solder temperature (10 s) (Note 5)		T <sub>sol</sub>	260	°C
Isolation voltage (AC, 1 minute, R.H. ≤ 60%) (Note 6)		BV <sub>S</sub>	2500	V <sub>rms</sub>

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: 50% duty cycle, 1 ms pulse width.

Note 2: Pulse width ≤ 1μs, 300 pps.

Note 3: 1 minute maximum.

Note 4: Not to exceed V<sub>CC</sub> by more than 500 mV.

Note 5: Soldering portion of lead: up to 2 mm from the body of the device.

Note 6: Device considered a two-terminal device: Pins 1, 2, 3 and 4 shorted together, and pins 5, 6, 7 and 8 shorted together.

## Recommended Operating Conditions

Characteristics	Symbol	Min	Typ.	Max	Unit
Input current, low level	I <sub>FL</sub>	0	—	250	μA
Input current, high level	I <sub>FH</sub>	7	—	20	mA
Supply voltage, output	V <sub>CC</sub>	4.5	—	5.5	V
High level enable voltage	V <sub>EH</sub>	2.0	—	V <sub>CC</sub>	V
Low level enable voltage	V <sub>EL</sub>	0	—	0.8	V
Fan out (TTL load)	N	—	—	8	—
Operating temperature	T <sub>opr</sub>	0	—	70	°C

Note: The recommended operating conditions are given as a design guideline to obtain expected performance of the device. In addition, each item is an independent guideline. In developing designs using this product, please confirm the specified characteristics shown in this document.

## Electrical Characteristics (unless otherwise specified, for 0°C ≤ Ta ≤ 70°C)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Input forward voltage	V <sub>F</sub>	I <sub>F</sub> = 10 mA, Ta = 25°C	—	1.65	1.8	V
Input diode temperature coefficient	ΔV <sub>F</sub> /ΔTa	I <sub>F</sub> = 10 mA	—	-2.0	—	mV/°C
Input reverse current	I <sub>R</sub>	V <sub>R</sub> = 5 V, Ta = 25°C	—	—	10	μA
Input capacitance	C <sub>T</sub>	V <sub>F</sub> = 0 V, f = 1 MHz, Ta = 25°C	—	45	—	pF
High level output current	I <sub>OH</sub>	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 5.5 V I <sub>F</sub> = 250 μA, V <sub>E</sub> = 2.0 V	—	10	250	μA
Low level output voltage	V <sub>OL</sub>	V <sub>CC</sub> = 5.5 V, I <sub>F</sub> = 5 mA V <sub>EH</sub> = 2.0 V, I <sub>OL</sub> = 13 mA (sinking)	—	0.4	0.6	V
Input current logic low output level	I <sub>FH</sub>	I <sub>OL</sub> = 13 mA (sinking), V <sub>O</sub> = 0.6 V, V <sub>CC</sub> = 5.5 V, V <sub>EH</sub> = 2.0 V	—	—	5	mA
High level enable current	I <sub>EH</sub>	V <sub>CC</sub> = 5.5 V, V <sub>E</sub> = 2.0 V	—	-1.0	—	mA
Low level enable current	I <sub>EL</sub>	V <sub>CC</sub> = 5.5 V, V <sub>E</sub> = 0.5 V	—	-1.6	-2.0	mA
High level supply current	I <sub>CC</sub> H	V <sub>CC</sub> = 5.5 V, I <sub>F</sub> = 0 mA, V <sub>E</sub> = 0.5 V	—	7	15	mA
Low level supply current	I <sub>CC</sub> L	V <sub>CC</sub> = 5.5 V, I <sub>F</sub> = 10 mA, V <sub>E</sub> = 0.5 V	—	12	18	mA
Current transfer ratio	CTR	I <sub>F</sub> = 5.0 mA, R <sub>L</sub> = 100 Ω V <sub>CC</sub> = 5.0 V, Ta = 25°C	—	1000	—	%
Resistance (input-output)	R <sub>S</sub>	V <sub>S</sub> = 500 V, R.H. ≤ 60%, Ta = 25°C	5 × 10 <sup>10</sup>	10 <sup>14</sup>	—	Ω
Capacitance (input-output)	C <sub>S</sub>	V <sub>S</sub> = 0 V, f = 1 MHz, Ta = 25°C	—	0.6	—	pF

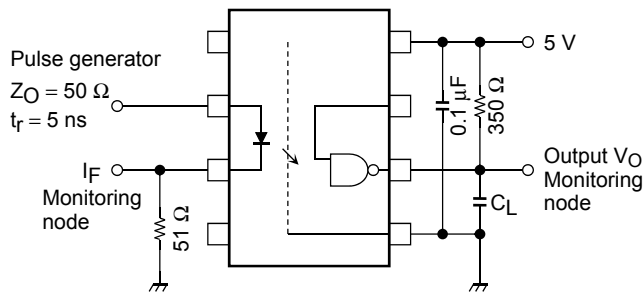
## Switching Characteristics (Ta = 25°C, V<sub>CC</sub> = 5 V)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Propagation delay time to high output level (L → H)	t <sub>pLH</sub>	1	R <sub>L</sub> = 350 Ω, C <sub>L</sub> = 15 pF I <sub>F</sub> = 7.5 mA	—	60	120	ns
Propagation delay time to low output level (H → L)	t <sub>pHL</sub>	1	R <sub>L</sub> = 350 Ω, C <sub>L</sub> = 15 pF I <sub>F</sub> = 7.5 mA	—	60	120	ns
Output rise fall time (10 to 90%)	t <sub>r</sub> , t <sub>f</sub>	1	R <sub>L</sub> = 350 Ω, C <sub>L</sub> = 15 pF I <sub>F</sub> = 7.5 mA	—	30	—	ns
Propagation delay time of enable from V <sub>EH</sub> to V <sub>EL</sub>	t <sub>ELH</sub>	2	R <sub>L</sub> = 350 Ω, C <sub>L</sub> = 15 pF I <sub>F</sub> = 7.5 mA, V <sub>EH</sub> = 3.0 V	—	25	—	ns
Propagation delay time of enable from V <sub>EL</sub> to V <sub>EH</sub>	t <sub>EHL</sub>	2	R <sub>L</sub> = 350 Ω, C <sub>L</sub> = 15 pF I <sub>F</sub> = 7.5 mA, V <sub>EH</sub> = 3.0 V	—	25	—	ns
Common mode transient immunity at logic high output level	CM <sub>H</sub>	3	V <sub>CM</sub> = 200 V, R <sub>L</sub> = 350 Ω V <sub>O</sub> (min) = 2 V, I <sub>F</sub> = 0 mA	—	200	—	V / μs
Common mode transient immunity at logic low output level	CM <sub>L</sub>	3	V <sub>CM</sub> = 200 V, R <sub>L</sub> = 350 Ω V <sub>O</sub> (max) = 0.8 V, I <sub>F</sub> = 5 mA	—	-500	—	V / μs

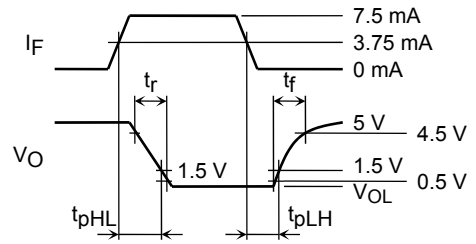
### Instruction for use

1. A ceramic capacitor (0.1 μF) should be connected from pin 8 and pin 5 to stabilize the operation of the high gain linear amplifier. Failure to provide the bypassing may impair the switching properties. The total lead length between the capacitor and coupler should not exceed 1 cm.
2. Maximum electrostatic discharge voltage for any pins: 180 V (C = 200 pF, R = 0).

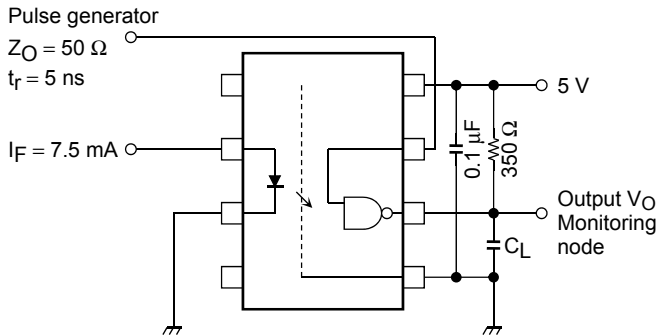
**Test Circuit 1: Switching Time Test Circuit**



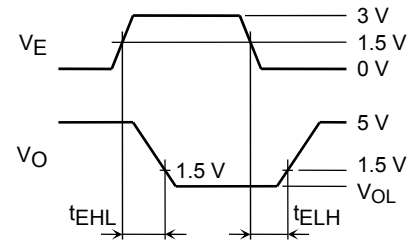
$C_L$  is approximately 15 pF which includes probe and stray wiring capacitance.



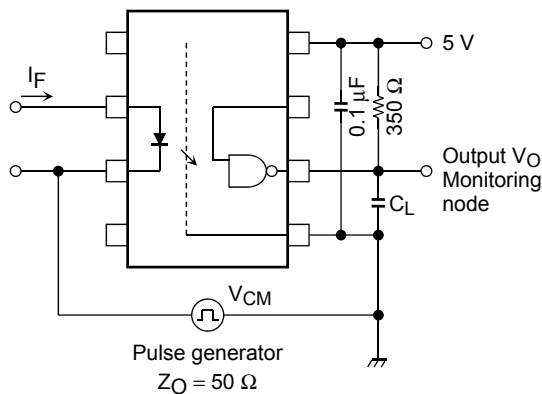
**Test Circuit 2: Switching Time Test Circuit**



$C_L$  is approximately 15 pF which includes probe and stray wiring capacitance.

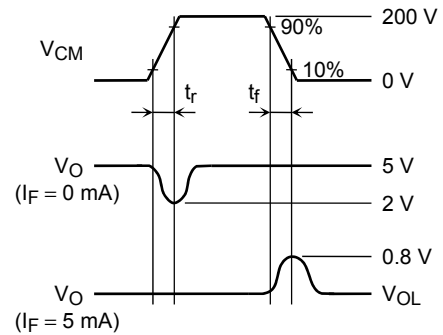


**Test Circuit 3: Common Mode Noise Immunity Test Circuit**



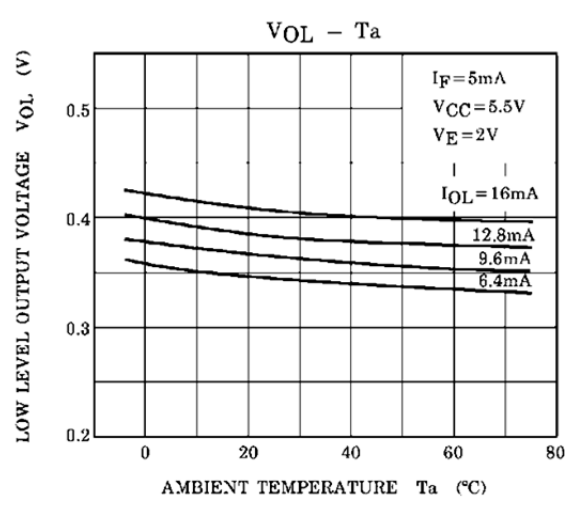
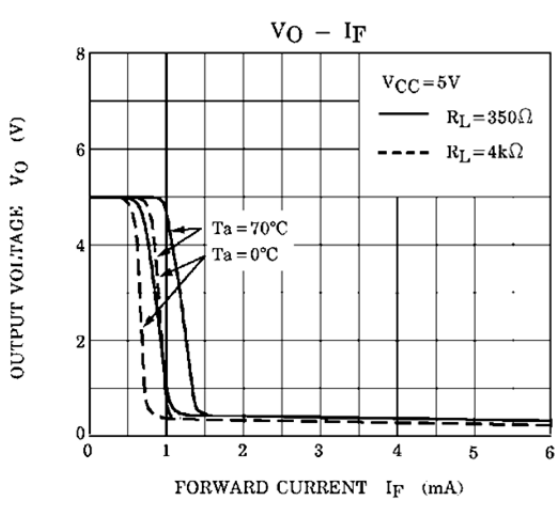
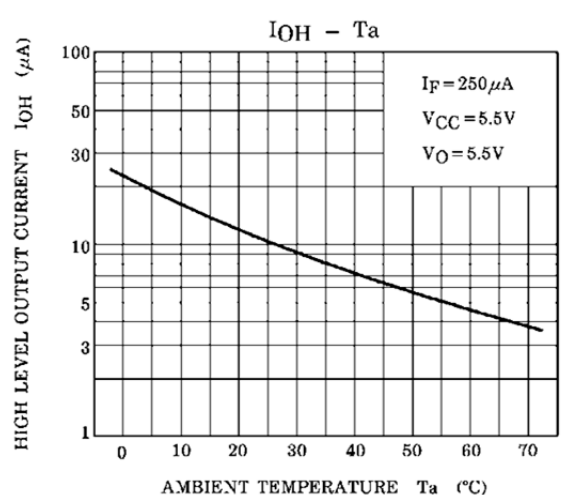
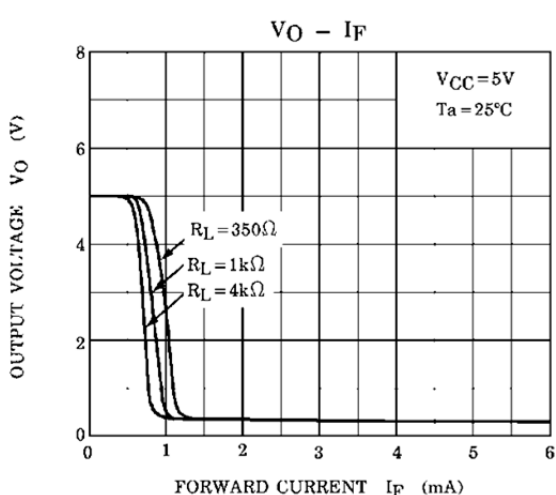
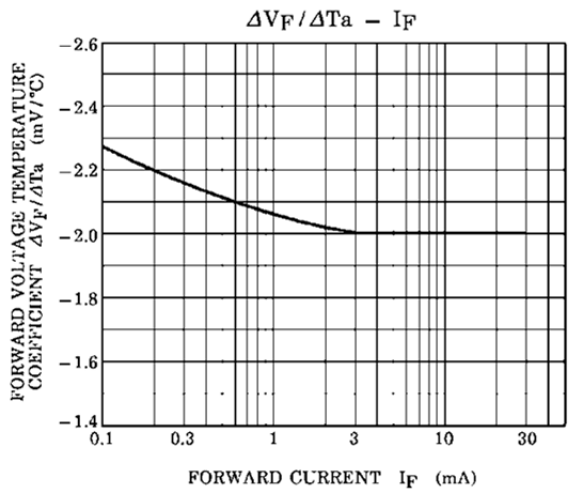
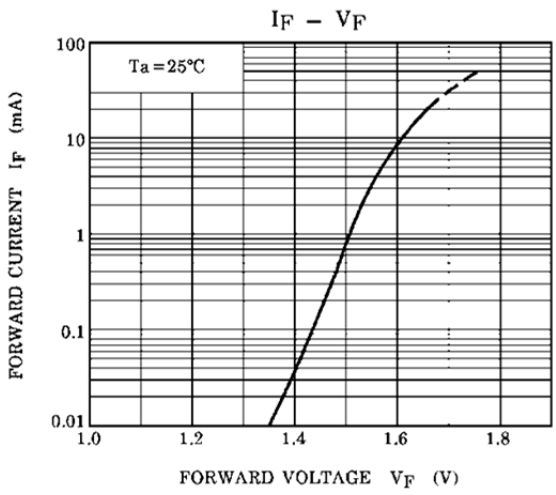
$$CM_H = \frac{160 \text{ (V)}}{t_r \text{ (}\mu\text{s)}}, CM_L = \frac{160 \text{ (V)}}{t_f \text{ (}\mu\text{s)}}$$

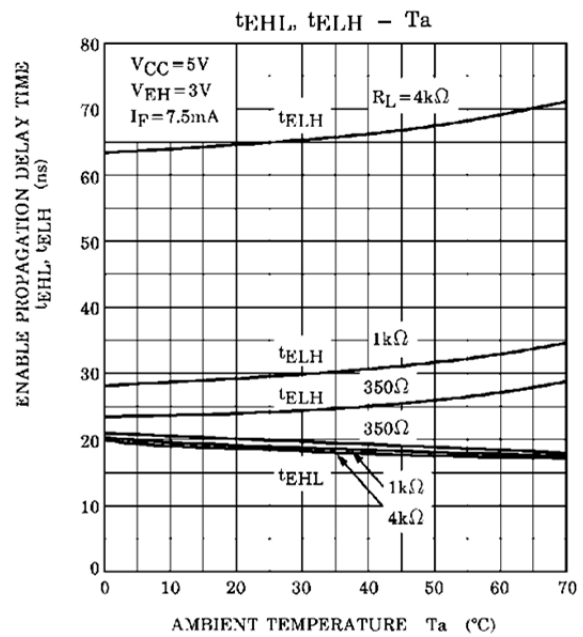
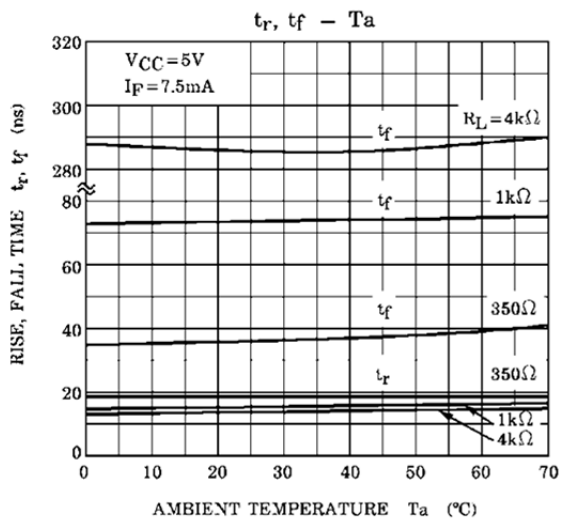
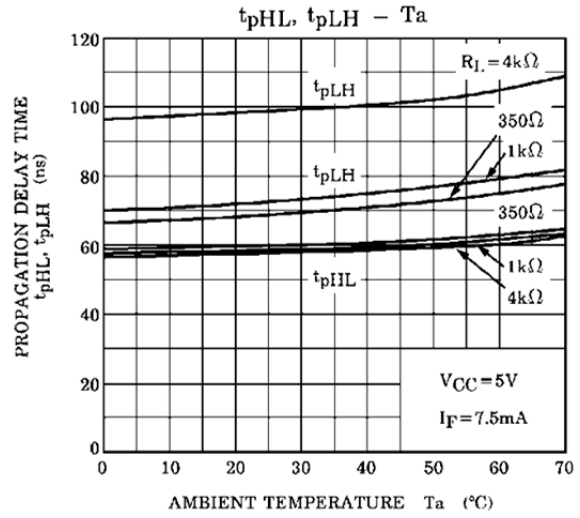
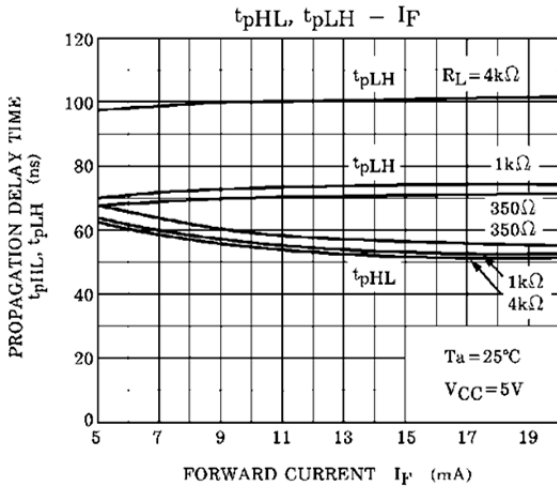
$C_L$  is approximately 15 pF which includes probe and stray wiring capacitance.



$CM_H$ : The maximum tolerable rate of rise of the common mode voltage to ensure the output will remain in the high output state (i.e.,  $V_O > 2.0 \text{ V}$ ). Measured in volts per microsecond ( $\text{V} / \mu\text{s}$ ).

$CM_L$ : The maximum tolerable rate of fall of the common mode voltage to ensure the output will remain in the low output state (i.e.,  $V_O < 0.8 \text{ V}$ ). Measured in volts per microsecond ( $\text{V} / \mu\text{s}$ ).





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