



QUAD DIGITAL ISOLATORS

FEATURES

- 1, 25, and 150-Mbps Signaling Rate Options
 - Low Channel-to-Channel Output Skew; 1 ns Max
 - Low Pulse-Width Distortion (PWD); 2 ns Max
 - Low Jitter Content; 1 ns Typ at 150 Mbps
- Typical 25-Year Life at Rated Working Voltage (see application note [SLLA197](#) and [Figure 15](#))
- 4000-V_{peak} Isolation, 560-V_{peak} Working Voltage
- UL 1577 Certified
- 4 kV ESD Protection
- Operate With 3.3-V or 5-V Supplies
- High Electromagnetic Immunity (see application report [SLLA181](#))
- –40°C to 125°C Operating Range

APPLICATIONS

- Industrial Fieldbus
- Computer Peripheral Interface
- Servo Control Interface
- Data Acquisition

DESCRIPTION

The ISO7240, ISO7241 and ISO7242 are quad-channel digital isolators with multiple channel configurations and output enable functions. These devices have logic input and output buffers separated by TI's silicon dioxide (SiO₂) isolation barrier. Used in conjunction with isolated power supplies, these devices block high voltage, isolate grounds, and prevent noise currents from entering the local ground and interfering with or damaging sensitive circuitry.

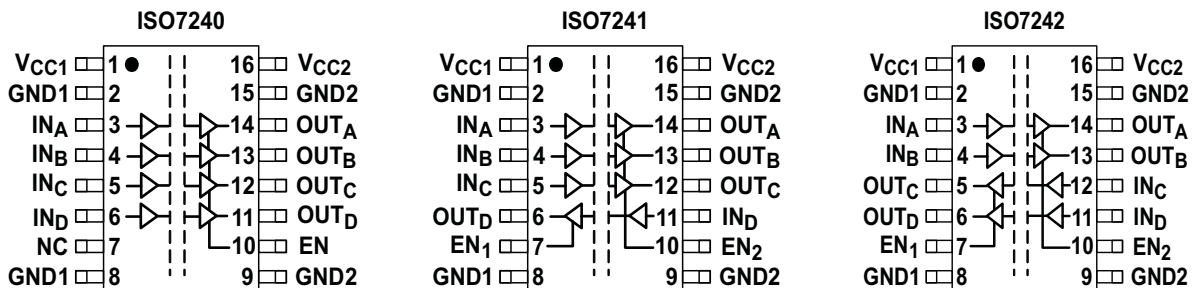
The ISO7240 has all four channels in the same direction while the ISO7241 has three channels the same direction and one channel in opposition. The ISO7242 has two channels in each direction.

The A and C option devices have TTL input thresholds and a noise-filter at the input that prevents transient pulses from being passed to the output of the device. The M option devices have CMOS V_{cc}/2 input thresholds and do not have the input noise-filter or the additional propagation delay.

A periodic update pulse is sent across the barrier to ensure the proper dc level of the output. If this dc-refresh pulse is not received, the input is assumed to be unpowered or not being actively driven, and the failsafe circuit drives the output to a logic high state. (Contact TI for a logic low failsafe option).

These devices may be powered from either 3.3-V or 5-V supplies on either side in any 3.3-V / 3.3-V, 5-V / 5-V, 5-V / 3.3-V, or 3.3-V / 5-V combination. Note that the signal input pins are 5-V tolerant regardless of the voltage supply level being used.

These devices are characterized for operation over the ambient temperature range of –40°C to 125°C.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

FUNCTION DIAGRAM

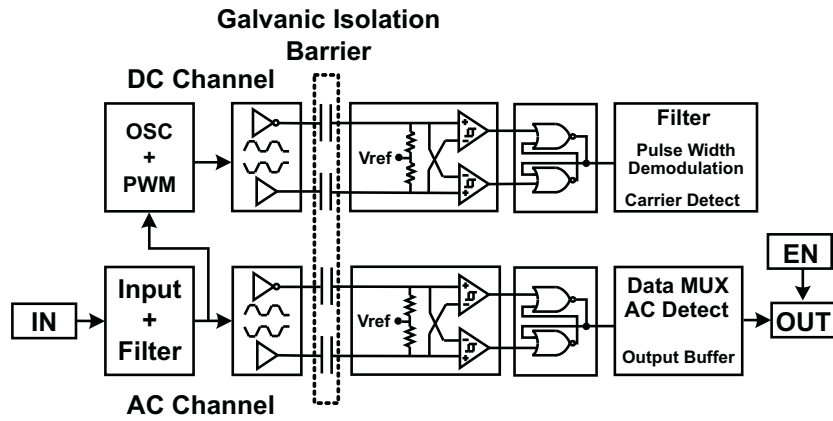


Table 1. Device Function Table ISO724x ⁽¹⁾

V _{CC1}	V _{CC2}	INPUT (IN)	OUTPUT ENABLE (EN)	OUTPUT (OUT)
PU	PU	H	H or Open	H
		L	H or Open	L
		X	L	Z
		Open	H or Open	H
PD	PU	X	H or Open	H
PD	PU	X	L	Z

(1) PU = Powered Up; PD = Powered Down ; X = Irrelevant; H = High Level; L = Low Level

AVAILABLE OPTIONS

PRODUCT	SIGNALING RATE	INPUT THRESHOLD	CHANNEL CONFIGURATION	MARKED AS	ORDERING NUMBER ⁽¹⁾
ISO7240ADW	1 Mbps	~1.5 V (TTL) (CMOS compatible)	4/0	ISO7240A	ISO7240ADW (rail)
					ISO7240ADWR (reel)
ISO7240CDW	25 Mbps	~1.5 V (TTL) (CMOS compatible)		ISO7240C	ISO7240CDW (rail)
					ISO7240CDWR (reel)
ISO7240MDW	150 Mbps	V _{cc} /2 (CMOS)		ISO7240M	ISO7240MDW (rail)
					ISO7240MDWR (reel)
ISO7241ADW	1 Mbps	~1.5 V (TTL) (CMOS compatible)	3/1	ISO7241A	ISO7241ADW (rail)
					ISO7241ADWR (reel)
ISO7241CDW	25 Mbps	~1.5 V (TTL) (CMOS compatible)		ISO7241C	ISO7241CDW (rail)
					ISO7241CDWR (reel)
ISO7241MDW	150 Mbps	V _{cc} /2 (CMOS)		ISO7241M	ISO7241MDW (rail)
					ISO7241MDWR (reel)
ISO7242ADW	1 Mbps	~1.5 V (TTL) (CMOS compatible)	2/2	ISO7242A	ISO7242ADW (rail)
					ISO7242ADWR (reel)
ISO7242CDW	25 Mbps	~1.5 V (TTL) (CMOS compatible)		ISO7242C	ISO7242CDW (rail)
					ISO7242CDWR (reel)
ISO7242MDW	150 Mbps	V _{cc} /2 (CMOS)		ISO7242M	ISO7242MDW (rail)
					ISO7242MDWR (reel)

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

			VALUE	UNIT	
V_{CC}	Supply voltage ⁽²⁾ , V_{CC1} , V_{CC2}		–0.5 to 6	V	
V_I	Voltage at IN, OUT, EN		–0.5 to 6	V	
I_O	Output current		±15	mA	
ESD	Electrostatic discharge	Human Body Model	JEDEC Standard 22, Test Method A114-C.01	±4	kV
		Field-Induced-Charged Device Model	JEDEC Standard 22, Test Method C101		
		Machine Model	ANSI/ESDS5.2-1996	±1	
T_J	Maximum junction temperature		±200	V	
			170	°C	

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to network ground terminal and are peak voltage values.

RECOMMENDED OPERATING CONDITIONS

			MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage, V_{CC1} , V_{CC2}		4.5		5.5	V
			3.15		3.45	
I_{OH}	High-level output current				4	mA
I_{OL}	Low-level output current		–4			mA
t_{ui}	Input pulse width	ISO724xA	1			µs
		ISO724xC	40			ns
		ISO724xM	6.67	5		
$1/t_{ui}$	Signaling rate	ISO724xA	0	1500 ⁽¹⁾	1000	kbps
		ISO724xC	0	30 ⁽¹⁾	25	Mbps
		ISO724xM	0	200 ⁽¹⁾	150	
V_{IH}	High-level input voltage (IN)	ISO724xM	0.7 V_{CC}		V_{CC}	V
V_{IL}	Low-level input voltage (IN)		0		0.3 V_{CC}	V
V_{IH}	High-level input voltage (IN) (EN on all devices)	ISO724xA, ISO724xC	2		V_{CC}	V
V_{IL}	Low-level input voltage (IN) (EN on all devices)		0		0.8	V
T_J	Junction temperature				150	°C
H	External magnetic field-strength immunity per IEC 61000-4-8 and IEC 61000-4-9 certification				1000	A/m

- (1) Typical value at room temperature and well-regulated power supply.

ELECTRICAL CHARACTERISTICS

V_{CC1} and V_{CC2} at 5-V operation, over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT	
SUPPLY CURRENT								
I_{CC1}	ISO7240A/C/M	Quiescent	$V_I = V_{CC}$ or 0 V, All channels, no load, EN_2 at 3 V		1	3	mA	
	ISO7240A	1 Mbps			1	3		
	ISO7240C/M	25 Mbps			7	10.5		
	ISO7241A/C/M	Quiescent	$V_I = V_{CC}$ or 0 V, All channels, no load, EN_1 at 3 V, EN_2 at 3 V		6.5	10	mA	
		ISO7241A		1 Mbps		6.5		10
		ISO7241C/M		25 Mbps		12		18
		ISO7242A/C/M		Quiescent		10		16
	ISO7242A	1 Mbps	$V_I = V_{CC}$ or 0 V, All channels, no load, EN_1 at 3 V, EN_2 at 3 V		10	16	mA	
		ISO7242C/M		25 Mbps		15		24
I_{CC2}	ISO7240A/C/M	Quiescent	$V_I = V_{CC}$ or 0 V, All channels, no load, EN_2 at 3 V		15	22	mA	
	ISO7240A	1 Mbps			16	22		
	ISO7240C/M	25 Mbps			17	25		
	ISO7241A/C/M	Quiescent	$V_I = V_{CC}$ or 0 V, All channels, no load, EN_1 at 3 V, EN_2 at 3 V		13	20	mA	
		ISO7241A		1 Mbps		13		20
		ISO7241C/M		25 Mbps		18		28
	ISO7242A/C/M	Quiescent	$V_I = V_{CC}$ or 0 V, All channels, no load, EN_1 at 3 V, EN_2 at 3 V		10	16	mA	
		ISO7242A		1 Mbps		10		16
		ISO7242C/M		25 Mbps		15		24
ELECTRICAL CHARACTERISTICS								
I_{OFF}	Sleep mode output current	EN at VCC, Single channel			0		μ A	
V_{OH}	High-level output voltage	$I_{OH} = -4$ mA, See Figure 1		$V_{CC} - 0.8$			V	
		$I_{OH} = -20$ μ A, See Figure 1		$V_{CC} - 0.1$				
V_{OL}	Low-level output voltage	$I_{OL} = 4$ mA, See Figure 1				0.4	V	
		$I_{OL} = 20$ μ A, See Figure 1				0.1		
$V_{I(HYS)}$	Input voltage hysteresis				150		mV	
I_{IH}	High-level input current	IN from 0 V to V_{CC}				10	μ A	
I_{IL}	Low-level input current					-10		
C_1	Input capacitance to ground	IN at V_{CC} , $V_I = 0.4 \sin(4E6\pi t)$			2		pF	
CMTI	Common-mode transient immunity	$V_I = V_{CC}$ or 0 V, See Figure 4			25	50	kV/ μ s	

SWITCHING CHARACTERISTICS

V_{CC1} and V_{CC2} at 5-V operation, over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH} , t_{PHL}	Propagation delay	See Figure 1	40		95	ns
PWD	Pulse-width distortion ⁽¹⁾ $ t_{PHL} - t_{PLH} $				10	
t_{PLH} , t_{PHL}	Propagation delay		18		42	ns
PWD	Pulse-width distortion ⁽¹⁾ $ t_{PHL} - t_{PLH} $				2.5	
t_{PLH} , t_{PHL}	Propagation delay		10		23	ns
PWD	Pulse-width distortion ⁽¹⁾ $ t_{PHL} - t_{PLH} $			1	2	
$t_{sk(o)}$	Channel-to-channel output skew ⁽²⁾	ISO724xA/C			2	ns
		ISO724xM		0	1	
t_r	Output signal rise time	See Figure 1		2		ns
t_f	Output signal fall time			2		
t_{PHZ}	Propagation delay, high-level-to-high-impedance output	See Figure 2		15	20	ns
t_{PZH}	Propagation delay, high-impedance-to-high-level output			15	20	
t_{PLZ}	Propagation delay, low-level-to-high-impedance output			15	20	
t_{PZL}	Propagation delay, high-impedance-to-low-level output			15	20	
t_{fs}	Failsafe output delay time from input power loss	See Figure 3		12		μ s
$t_{jit(pp)}$	Peak-to-peak eye-pattern jitter	ISO724xM	150 Mbps NRZ data input, Same polarity input on all channels, See Figure 5		1	ns

(1) Also referred to as pulse skew.

(2) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

ELECTRICAL CHARACTERISTICS

V_{CC1} at 5-V, V_{CC2} at 3.3-V operation, over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT	
SUPPLY CURRENT								
I_{CC1}	ISO7240A/C/M	Quiescent	$V_1 = V_{CC}$ or 0 V, All channels, no load, EN_2 at 3 V		1	3	mA	
	ISO7240A	1 Mbps			1	3		
	ISO7240C/M	25 Mbps			7	10.5		
	ISO7241A/C/M	Quiescent	$V_1 = V_{CC}$ or 0 V, All channels, no load, EN_1 at 3 V, EN_2 at 3 V		6.5	10	mA	
		ISO7241A		1 Mbps		6.5		10
		ISO7241C/M		25 Mbps		12		18
	ISO7242A/C/M	Quiescent	$V_1 = V_{CC}$ or 0 V, All channels, no load, EN_1 at 3 V, EN_2 at 3 V		10	16	mA	
		ISO7242A		1 Mbps		10		16
		ISO7242C/M		25 Mbps		15		24
I_{CC2}	ISO7240A/C/M	Quiescent	$V_1 = V_{CC}$ or 0 V, All channels, no load, EN_2 at 3 V		9.5	15	mA	
	ISO7240A	1 Mbps			10	15		
	ISO7240C/M	25 Mbps			10.5	17		
	ISO7241A/C/M	Quiescent	$V_1 = V_{CC}$ or 0 V, All channels, no load, EN_1 at 3 V, EN_2 at 3 V		8	13	mA	
		ISO7241A		1 Mbps		8		13
		ISO7241C/M		25 Mbps		11.5		18
	ISO7242A/C/M	Quiescent	$V_1 = V_{CC}$ or 0 V, All channels, no load, EN_1 at 3 V, EN_2 at 3 V		6	10	mA	
		ISO7242A		1 Mbps		6		10
		ISO7242C/M		25 Mbps		9		14
ELECTRICAL CHARACTERISTICS								
I_{OFF}	Sleep mode output current	EN at V_{CC} , Single channel			0		μ A	
V_{OH}	High-level output voltage	$I_{OH} = -4$ mA, See Figure 1	ISO7240	$V_{CC} - 0.4$		V		
			ISO724x (5-V side)	$V_{CC} - 0.8$				
				$V_{CC} - 0.1$				
V_{OL}	Low-level output voltage	$I_{OL} = 4$ mA, See Figure 1			0.4	V		
							0.1	
$V_{I(HYS)}$	Input voltage hysteresis				150		mV	
I_{IH}	High-level input current	IN from 0 V to V_{CC}				10	μ A	
I_{IL}	Low-level input current				-10			
C_I	Input capacitance to ground	IN at V_{CC} , $V_I = 0.4 \sin(4E6\pi t)$				2	pF	
CMTI	Common-mode transient immunity	$V_1 = V_{CC}$ or 0 V, See Figure 4			25	50	kV/ μ s	

SWITCHING CHARACTERISTICS

V_{CC1} at 5-V, V_{CC2} at 3.3-V operation, over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH} , t_{PHL}	Propagation delay	See Figure 1	40		100	ns
PWD	Pulse-width distortion ⁽¹⁾ $ t_{PHL} - t_{PLH} $				11	
t_{PLH} , t_{PHL}	Propagation delay		20		50	ns
PWD	Pulse-width distortion ⁽¹⁾ $ t_{PHL} - t_{PLH} $				3	
t_{PLH} , t_{PHL}	Propagation delay		12		29	ns
PWD	Pulse-width distortion ⁽¹⁾ $ t_{PHL} - t_{PLH} $			1	2	
$t_{sk(o)}$	Channel-to-channel output skew ⁽²⁾	ISO724xA/C			3	ns
		ISO724xM			0	1
t_r	Output signal rise time	See Figure 1		2		ns
t_f	Output signal fall time			2		
t_{PHZ}	Propagation delay, high-level-to-high-impedance output	See Figure 2		15	20	ns
t_{PZH}	Propagation delay, high-impedance-to-high-level output			15	20	
t_{PLZ}	Propagation delay, low-level-to-high-impedance output			15	20	
t_{PZL}	Propagation delay, high-impedance-to-low-level output			15	20	
t_{fs}	Failsafe output delay time from input power loss	See Figure 3		18		μ s
$t_{jit(pp)}$	Peak-to-peak eye-pattern jitter	ISO724xM	150 Mbps PRBS NRZ data input, Same polarity input on all channels, See Figure 5		1	ns

(1) Also known as pulse skew

(2) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

ELECTRICAL CHARACTERISTICS

V_{CC1} at 3.3-V, V_{CC2} at 5-V operation, over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY CURRENT								
I_{CC1}	ISO7240A/C/M	Quiescent	$V_I = V_{CC}$ or 0 V, All channels, no load, EN_2 at 3 V		0.5	1		mA
	ISO7240A	1 Mbps			1	2		
	ISO7240C/M	25 Mbps			3	5		
	ISO7241A/C/M	Quiescent	$V_I = V_{CC}$ or 0 V, All channels, no load, EN_1 at 3 V, EN_2 at 3 V		4	7		mA
	ISO7241A	1 Mbps			4	7		
	ISO7241C/M	25 Mbps			6.5	11		
	ISO7242A/C/M	Quiescent	$V_I = V_{CC}$ or 0 V, All channels, no load, EN_1 at 3 V, EN_2 at 3 V		6	10		mA
	ISO7242A	1 Mbps			6	10		
	ISO7242C/M	25 Mbps			9	14		
I_{CC2}	ISO7240A/C/M	Quiescent	$V_I = V_{CC}$ or 0 V, All channels, no load, EN_2 at 3 V		15	22		mA
	ISO7240A	1 Mbps			16	22		
	ISO7240C/M	25 Mbps			17	25		
	ISO7241A/C/M	Quiescent	$V_I = V_{CC}$ or 0 V, All channels, no load, EN_1 at 3 V, EN_2 at 3 V		13	20		mA
	ISO7241A	1 Mbps			13	20		
	ISO7241C/M	25 Mbps			18	28		
	ISO7242A/C/M	Quiescent	$V_I = V_{CC}$ or 0 V, All channels, no load, EN_1 at 3 V, EN_2 at 3 V		10	16		mA
	ISO7242A	1 Mbps			10	16		
	ISO7242C/M	25 Mbps			15	24		
ELECTRICAL CHARACTERISTICS								
I_{OFF}	Sleep mode output current	EN at VCC, Single channel			0			μ A
V_{OH}	High-level output voltage		$I_{OH} = -4$ mA, See Figure 1	ISO7240	$V_{CC} - 0.4$			V
				ISO724x (5-V side)	$V_{CC} - 0.8$			
					$V_{CC} - 0.1$			
V_{OL}	Low-level output voltage		$I_{OL} = 4$ mA, See Figure 1			0.4		V
							0.1	
$V_{I(HYS)}$	Input voltage hysteresis				150			mV
I_{IH}	High-level input current	IN from 0 V to V_{CC}				10		μ A
I_{IL}	Low-level input current				-10			
C_I	Input capacitance to ground	IN at V_{CC} , $V_I = 0.4 \sin(4E6\pi t)$				2		pF
CMTI	Common-mode transient immunity	$V_I = V_{CC}$ or 0 V, See Figure 4			25	50		kV/ μ s

SWITCHING CHARACTERISTICS

V_{CC1} at 3.3-V and V_{CC2} at 5-V operation, over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
t_{PLH} , t_{PHL}	Propagation delay	See Figure 1	40		100	ns	
PWD	Pulse-width distortion ⁽¹⁾ $ t_{PHL} - t_{PLH} $				11		
t_{PLH} , t_{PHL}	Propagation delay		22		51	ns	
PWD	Pulse-width distortion ⁽¹⁾ $ t_{PHL} - t_{PLH} $				3		
t_{PLH} , t_{PHL}	Propagation delay		ISO724xM	12		30	ns
PWD	Pulse-width distortion ⁽¹⁾ $ t_{PHL} - t_{PLH} $					1	
$t_{sk(o)}$	Channel-to-channel output skew ⁽²⁾	ISO724xA/C			2.5	ns	
		ISO724xM			0		1
t_r	Output signal rise time	See Figure 1		2		ns	
t_f	Output signal fall time			2			
t_{PHZ}	Propagation delay, high-level-to-high-impedance output	See Figure 2		15	20	ns	
t_{PZH}	Propagation delay, high-impedance-to-high-level output			15	20		
t_{PLZ}	Propagation delay, low-level-to-high-impedance output			15	20		
t_{PZL}	Propagation delay, high-impedance-to-low-level output			15	20		
t_{fs}	Failsafe output delay time from input power loss	See Figure 3		12		μ s	
$t_{jit(pp)}$	Peak-to-peak eye-pattern jitter	ISO724xM	150 Mbps NRZ data input, Same polarity input on all channels, See Figure 5		1	ns	

(1) Also known as pulse skew

(2) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

ELECTRICAL CHARACTERISTICS

V_{CC1} and V_{CC2} at 3.3 V operation, over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
I_{CC1}	ISO7240A/C/M	Quiescent	$V_1 = V_{CC}$ or 0 V, all channels, no load, EN_2 at 3 V	0.5	1	mA
	ISO7240A	1 Mbps		1	2	
	ISO7240C/M	25 Mbps		3	5	
	ISO7241A/C/M	Quiescent	$V_1 = V_{CC}$ or 0 V, all channels, no load, EN_1 at 3 V, EN_2 at 3 V	4	7	mA
	ISO7241A	1 Mbps		4	7	
	ISO7241C/M	25 Mbps		6.5	11	
	ISO7242A/C/M	Quiescent		6	10	
	ISO7242A	1 Mbps	$V_1 = V_{CC}$ or 0 V, all channels, no load, EN_1 at 3 V, EN_2 at 3 V	6	10	mA
ISO7242C/M	25 Mbps	9		14		
I_{CC2}	ISO7240A/C/M	Quiescent	$V_1 = V_{CC}$ or 0 V, all channels, no load, EN_2 at 3 V	9.5	15	mA
	ISO7240A	1 Mbps		10	15	
	ISO7240C/M	25 Mbps		10.5	17	
	ISO7241A/C/M	Quiescent	$V_1 = V_{CC}$ or 0 V, all channels, no load, EN_1 at 3 V, EN_2 at 3 V	8	13	mA
	ISO7241A	1 Mbps		8	13	
	ISO7241C/M	25 Mbps		11.5	18	
	ISO7242A/C/M	Quiescent		6	10	
	ISO7242A	1 Mbps	$V_1 = V_{CC}$ or 0 V, all channels, no load, EN_1 at 3 V, EN_2 at 3 V	6	10	mA
ISO7242C/M	25 Mbps	9		14		
ELECTRICAL CHARACTERISTICS						
I_{OFF}	Sleep mode output current	EN at V_{CC} , single channel		0		μ A
V_{OH}	High-level output voltage	$I_{OH} = -4$ mA, See Figure 1	$V_{CC} - 0.4$			V
		$I_{OH} = -20$ μ A, See Figure 1	$V_{CC} - 0.1$			
V_{OL}	Low-level output voltage	$I_{OL} = 4$ mA, See Figure 1			0.4	V
		$I_{OL} = 20$ μ A, See Figure 1			0.1	
$V_{I(HYS)}$	Input voltage hysteresis			150		mV
I_{IH}	High-level input current	IN from 0 V or V_{CC}			10	μ A
I_{IL}	Low-level input current				-10	
C_1	Input capacitance to ground	IN at V_{CC} , $V_1 = 0.4 \sin(4E6\pi t)$		2		pF
CMTI	Common-mode transient immunity	$V_1 = V_{CC}$ or 0 V, See Figure 4	25	50		kV/ μ s

SWITCHING CHARACTERISTICS

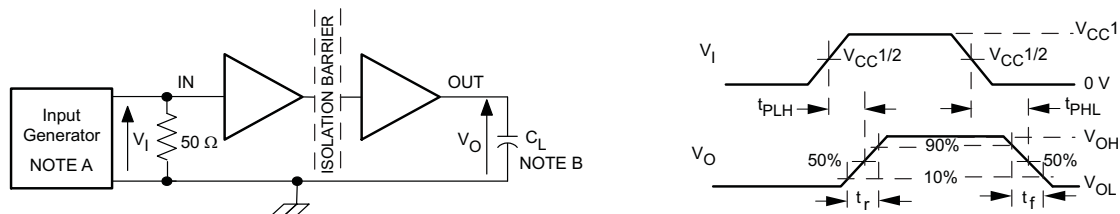
V_{CC1} and V_{CC2} at 3.3-V operation, over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
t_{PLH} , t_{PHL}	Propagation delay	See Figure 1	45		110	ns	
PWD	Pulse-width distortion $ t_{PHL} - t_{PLH} ^{(1)}$				12		
t_{PLH} , t_{PHL}	Propagation delay		25		56	ns	
PWD	Pulse-width distortion $ t_{PHL} - t_{PLH} ^{(1)}$				4		
t_{PLH} , t_{PHL}	Propagation delay		12		34	ns	
PWD	Pulse-width distortion $ t_{PHL} - t_{PLH} ^{(1)}$			1	2		
$t_{sk(o)}$	Channel-to-channel output skew ⁽²⁾	ISO724xA/C			3.5	ns	
		ISO724xM		0	1		
t_r	Output signal rise time	See Figure 1		2			
t_f	Output signal fall time			2			
t_{PHZ}	Propagation delay, high-level-to-high-impedance output	See Figure 2		15	20	ns	
t_{PZH}	Propagation delay, high-impedance-to-high-level output			15	20		
t_{PLZ}	Propagation delay, low-level-to-high-impedance output			15	20		
t_{PZL}	Propagation delay, high-impedance-to-low-level output			15	20		
t_{fs}	Failsafe output delay time from input power loss	See Figure 3		18		μ s	
$t_{jit(pp)}$	Peak-to-peak eye-pattern jitter	ISO724xM	150 Mbps PRBS NRZ data input, same polarity input on all channels, See Figure 5			1	ns

(1) Also referred to as pulse skew.

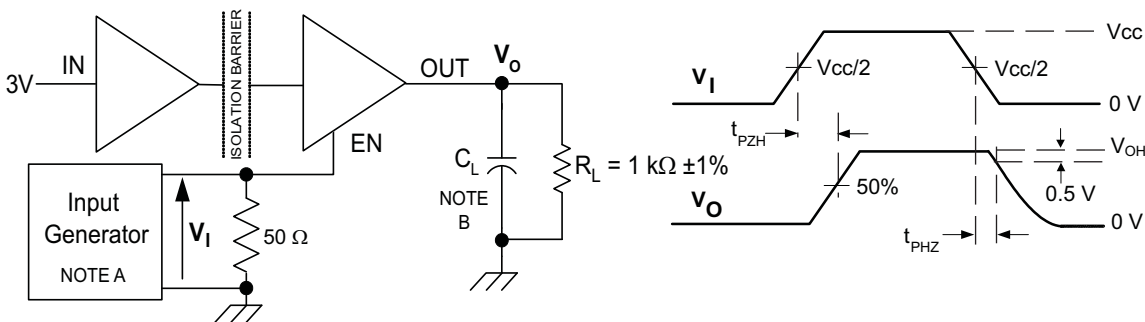
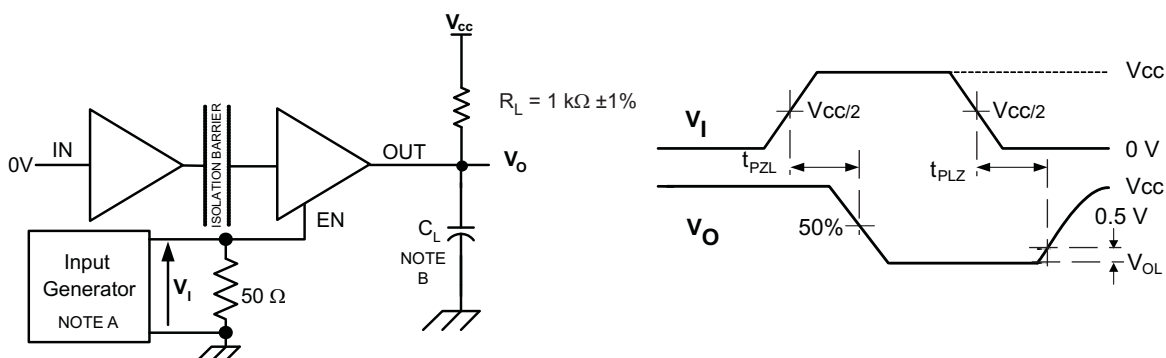
(2) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

PARAMETER MEASUREMENT INFORMATION



- The input pulse is supplied by a generator having the following characteristics: PRR \leq 50 kHz, 50% duty cycle, $t_r \leq$ 3 ns, $t_f \leq$ 3 ns, $Z_O = 50 \Omega$.
- $C_L = 15$ pF and includes instrumentation and fixture capacitance within $\pm 20\%$.

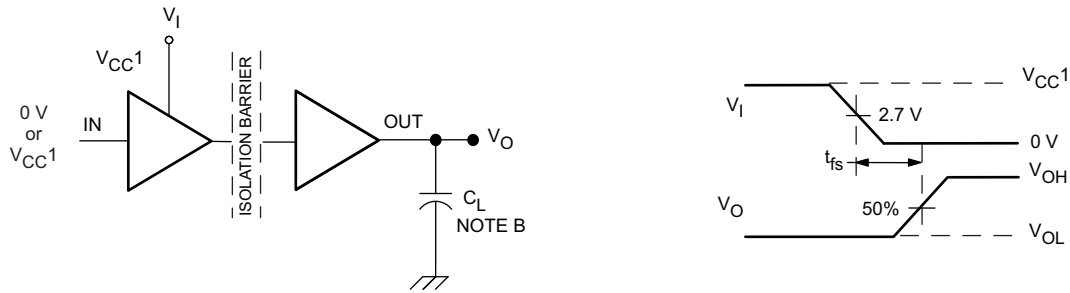
Figure 1. Switching Characteristic Test Circuit and Voltage Waveforms



- The input pulse is supplied by a generator having the following characteristics: PRR \leq 50 kHz, 50% duty cycle, $t_r \leq$ 3 ns, $t_f \leq$ 3 ns, $Z_O = 50 \Omega$.
- $C_L = 15$ pF and includes instrumentation and fixture capacitance within $\pm 20\%$.

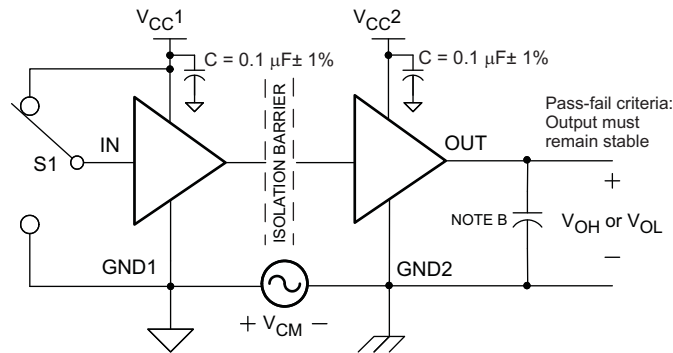
Figure 2. Enable/Disable Propagation Delay Time Test Circuit and Waveform

PARAMETER MEASUREMENT INFORMATION (continued)



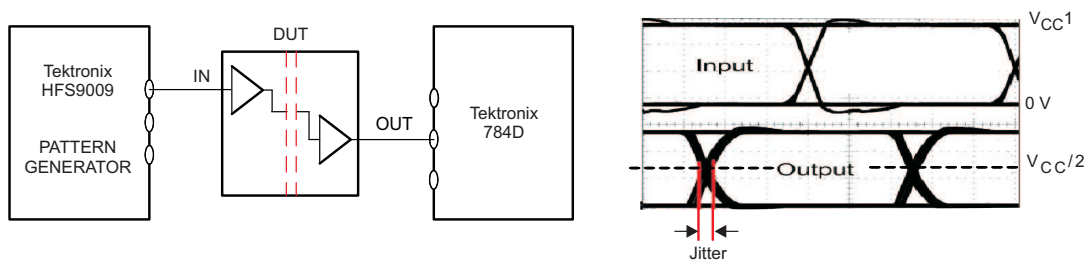
- A. $C_L = 15 \text{ pF}$ and includes instrumentation and fixture capacitance within $\pm 20\%$.
- B. The input pulse is supplied by a generator having the following characteristics: $\text{PRR} \leq 50 \text{ kHz}$, 50% duty cycle, $t_r \leq 3 \text{ ns}$, $t_f \leq 3 \text{ ns}$, $Z_O = 50 \Omega$.

Figure 3. Failsafe Delay Time Test Circuit and Voltage Waveforms



- A. $C_L = 15 \text{ pF}$ and includes instrumentation and fixture capacitance within $\pm 20\%$.
- B. The input pulse is supplied by a generator having the following characteristics: $\text{PRR} \leq 50 \text{ kHz}$, 50% duty cycle, $t_r \leq 3 \text{ ns}$, $t_f \leq 3 \text{ ns}$, $Z_O = 50 \Omega$.

Figure 4. Common-Mode Transient Immunity Test Circuit and Voltage Waveform



NOTE: PRBS bit pattern run length is $2^{16} - 1$. Transition time is 800 ps. NRZ data input has no more than five consecutive 1s or 0s.

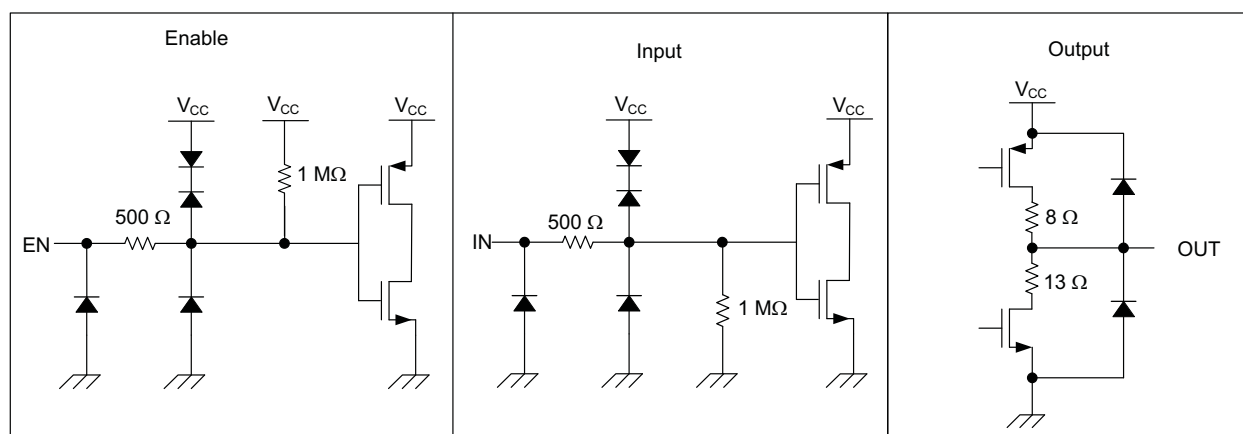
Figure 5. Peak-to-Pek Eye-Pattern Jitter Test Circuit and Voltage Waveform

DEVICE INFORMATION

PACKAGE CHARACTERISTICS

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
L(I01)	Minimum air gap (Clearance)	Shortest terminal-to-terminal distance through air	7.7			mm
L(I02)	Minimum external tracking (Creepage)	Shortest terminal-to-terminal distance across the package surface	8.1			mm
	Minimum Internal Gap (Internal Clearance)	Distance through the insulation	0.008			mm
R_{IO}	Isolation resistance	Input to output, $V_{IO} = 500\text{ V}$, all pins on each side of the barrier tied together creating a two-terminal device		$>10^{12}$		Ω
C_{IO}	Barrier capacitance Input to output	$V_1 = 0.4 \sin(4E6\pi t)$		2		pF
C_I	Input capacitance to ground	$V_1 = 0.4 \sin(4E6\pi t)$		2		pF

DEVICE I/O SCHEMATICS



REGULATORY INFORMATION

VDE	CSA	UL
Certified according to IEC 60747-5-2	Approved under CSA Component Acceptance Notice	Recognized under 1577 Component Recognition Program ⁽¹⁾
File Number: Pending	File Number: Pending	File Number: E181974

(1) Production tested ≥ 3000 Vrms for 1 second in accordance with UL 1577.

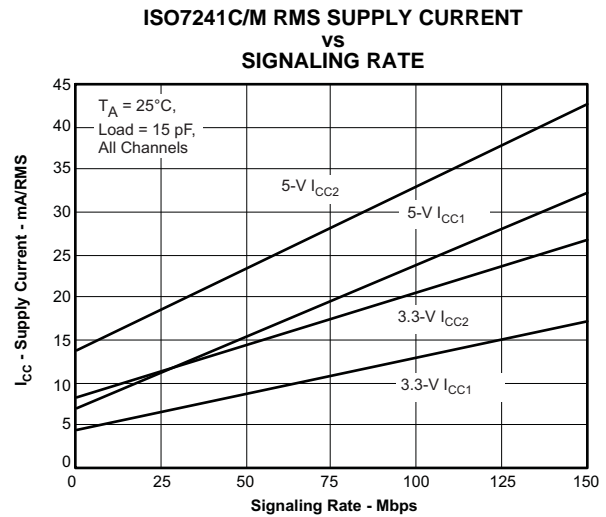
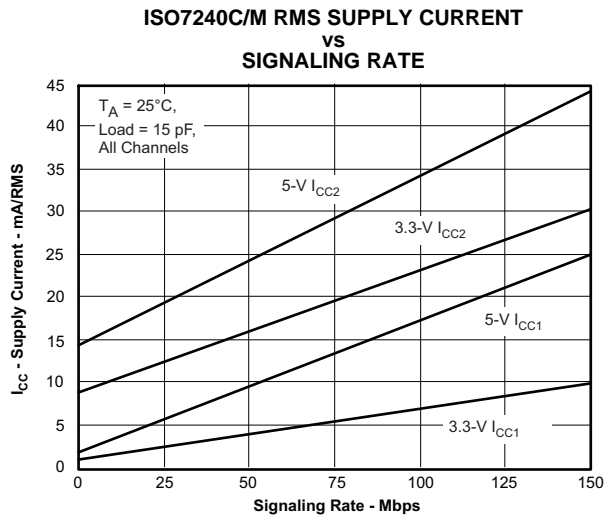
THERMAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
θ_{JA} Junction-to-air	Low-K Thermal Resistance ⁽¹⁾		168		°C/W
	High-K Thermal Resistance		96.1		
θ_{JB} Junction-to-Board Thermal Resistance			61		°C/W
θ_{JC} Junction-to-Case Thermal Resistance			48		°C/W
P_D Device Power Dissipation	$V_{CC1} = V_{CC2} = 5.5$ V, $T_J = 150^\circ\text{C}$, $C_L = 15$ pF, Input a 50% duty cycle square wave			220	mW

(1) Tested in accordance with the Low-K or High-K thermal metric definitions of EIA/JESD51-3 for leaded surface mount packages.

TYPICAL CHARACTERISTIC CURVES



TYPICAL CHARACTERISTIC CURVES (continued)

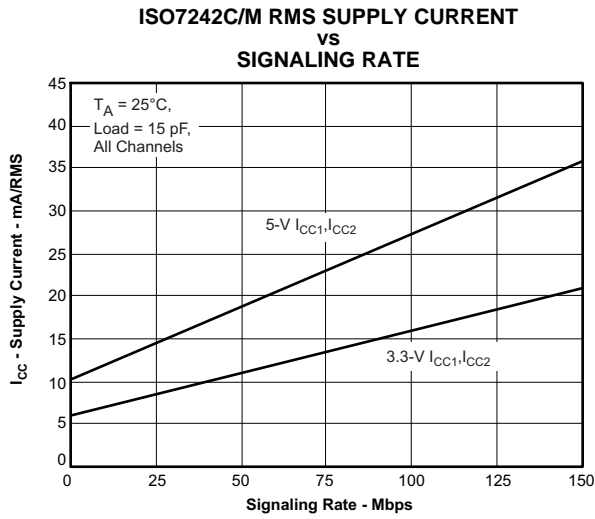


Figure 8.

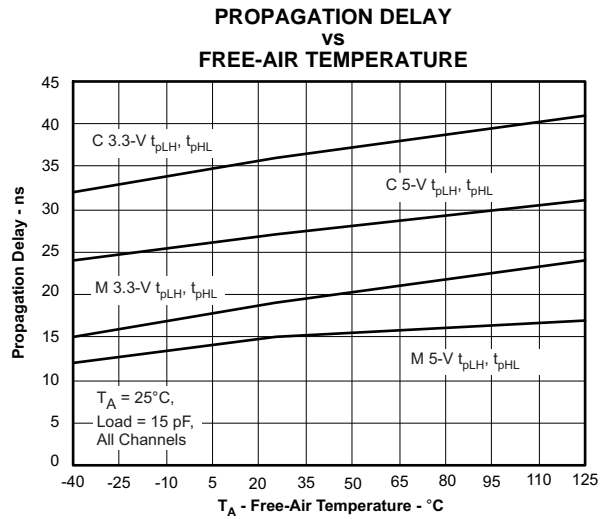


Figure 9.

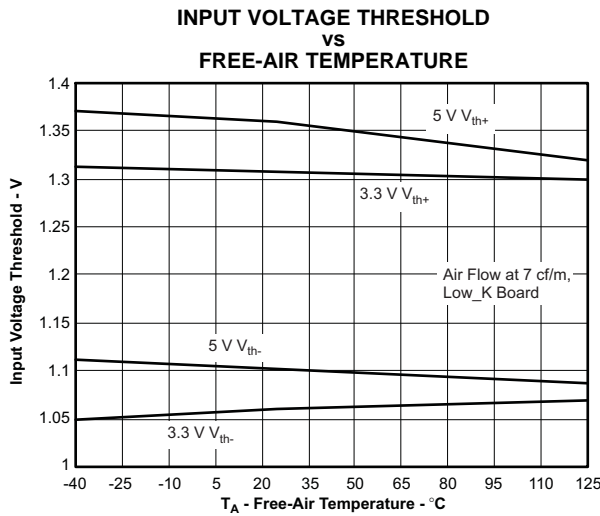


Figure 10.

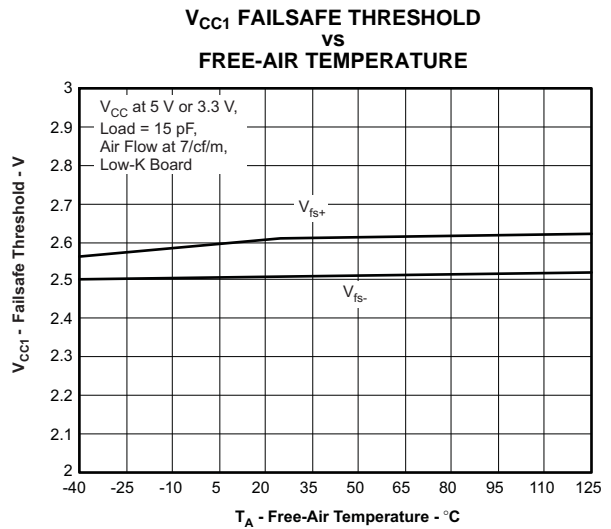
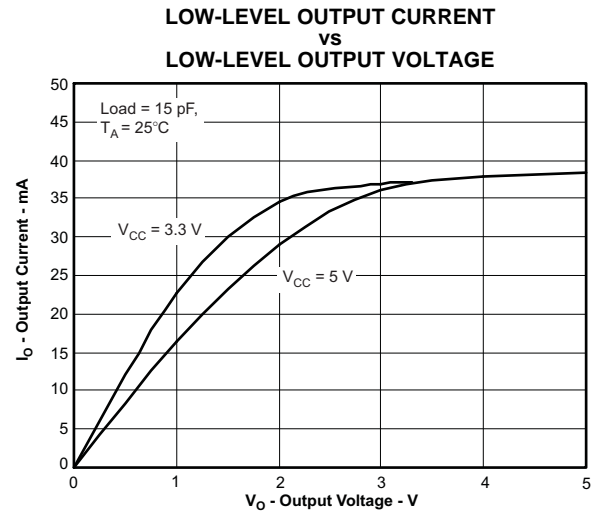
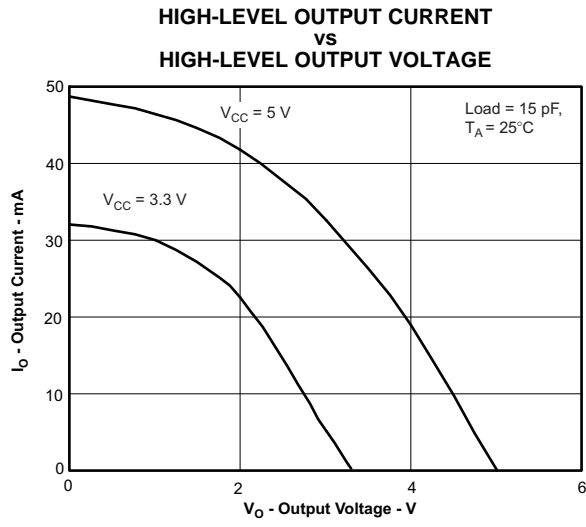


Figure 11.

TYPICAL CHARACTERISTIC CURVES (continued)



APPLICATION INFORMATION

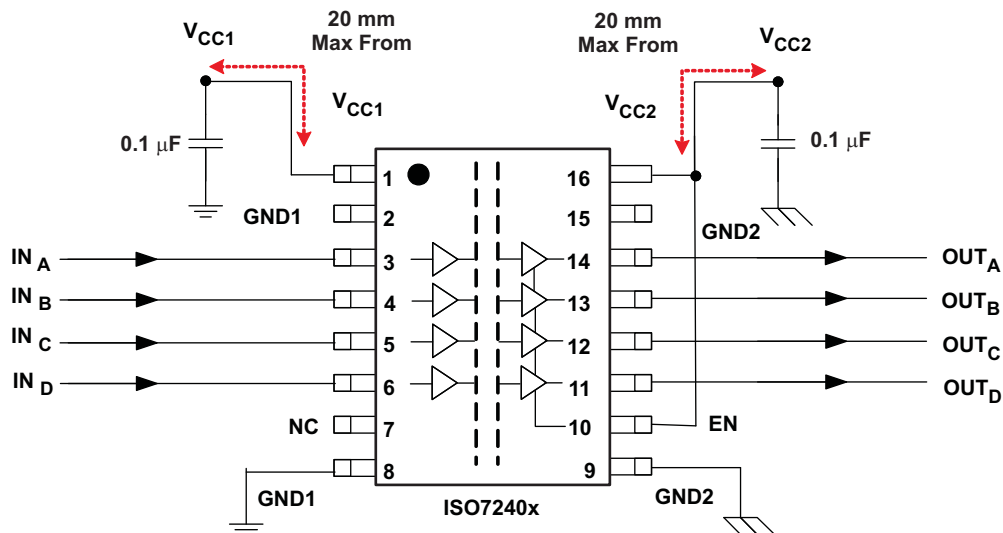


Figure 14. Typical ISO724x Application Circuit

LIFE EXPECTANCY vs. WORKING VOLTAGE

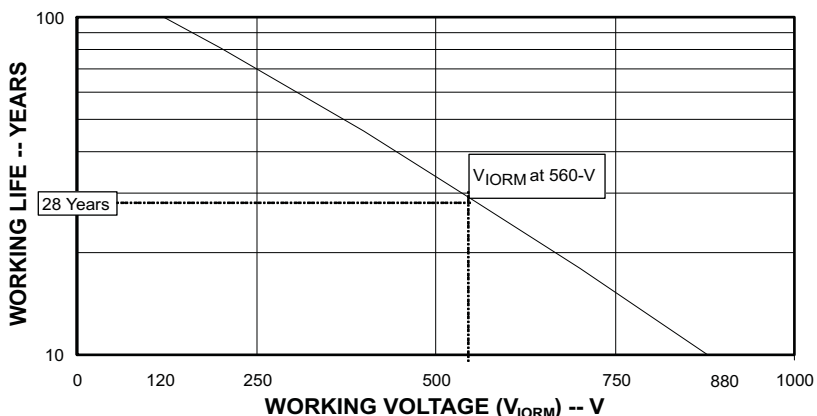


Figure 15. Time-Dependant Dielectric Breakdown Testing Results

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
ISO7240ADW	ACTIVE	SOIC	DW	16	49	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ISO7240ADWG4	ACTIVE	SOIC	DW	16	49	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ISO7240ADWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ISO7240ADWRG4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ISO7240CDW	ACTIVE	SOIC	DW	16	49	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ISO7240CDWG4	ACTIVE	SOIC	DW	16	49	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ISO7240CDWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ISO7240CDWRG4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ISO7240MDW	ACTIVE	SOIC	DW	16	49	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ISO7240MDWG4	ACTIVE	SOIC	DW	16	49	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ISO7240MDWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ISO7240MDWRG4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ISO7241ADW	ACTIVE	SOIC	DW	16	49	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ISO7241ADWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ISO7241CDW	ACTIVE	SOIC	DW	16	49	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ISO7241CDWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ISO7241MDW	ACTIVE	SOIC	DW	16	49	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ISO7241MDWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ISO7242ADW	ACTIVE	SOIC	DW	16	49	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ISO7242ADWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ISO7242CDW	ACTIVE	SOIC	DW	16	49	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ISO7242CDWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ISO7242MDW	ACTIVE	SOIC	DW	16	49	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ISO7242MDWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

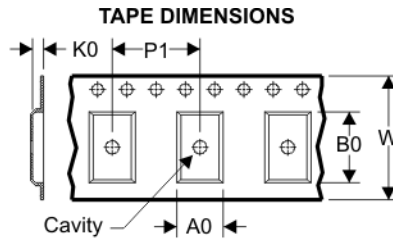
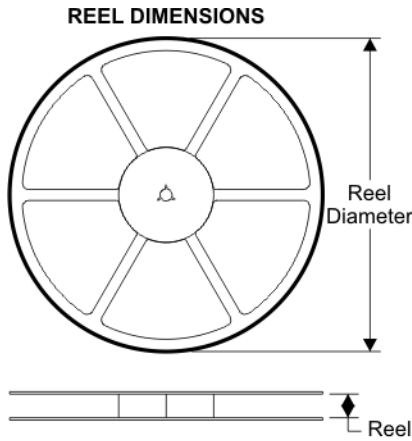
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

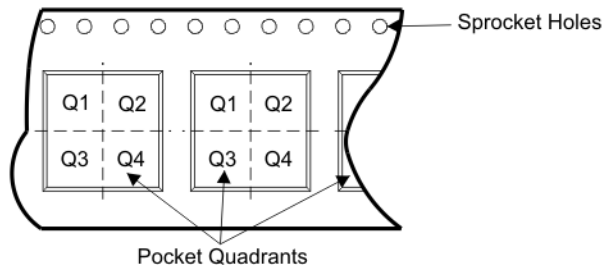
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL BOX INFORMATION



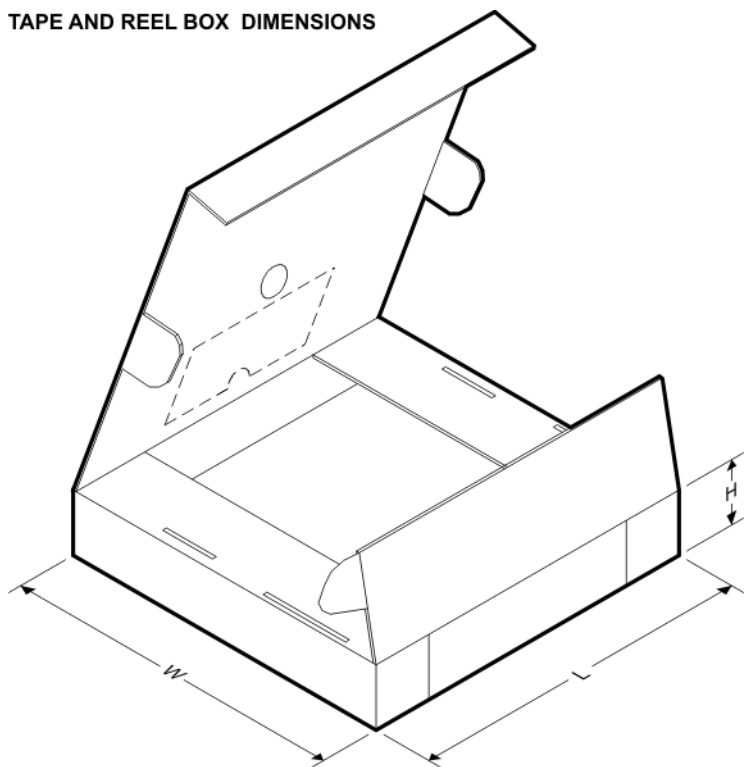
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO7240ADWR	DW	16	SITE 35	330	16	10.9	10.78	3.0	12	16	Q1
ISO7240CDWR	DW	16	SITE 35	330	16	10.9	10.78	3.0	12	16	Q1
ISO7240MDWR	DW	16	SITE 35	330	16	10.9	10.78	3.0	12	16	Q1
ISO7241ADWR	DW	16	SITE 35	330	16	10.9	10.78	3.0	12	16	Q1
ISO7241CDWR	DW	16	SITE 35	330	16	10.9	10.78	3.0	12	16	Q1
ISO7241MDWR	DW	16	SITE 35	330	16	10.9	10.78	3.0	12	16	Q1
ISO7242ADWR	DW	16	SITE 35	330	16	10.9	10.78	3.0	12	16	Q1
ISO7242CDWR	DW	16	SITE 35	330	16	10.9	10.78	3.0	12	16	Q1
ISO7242MDWR	DW	16	SITE 35	330	16	10.9	10.78	3.0	12	16	Q1

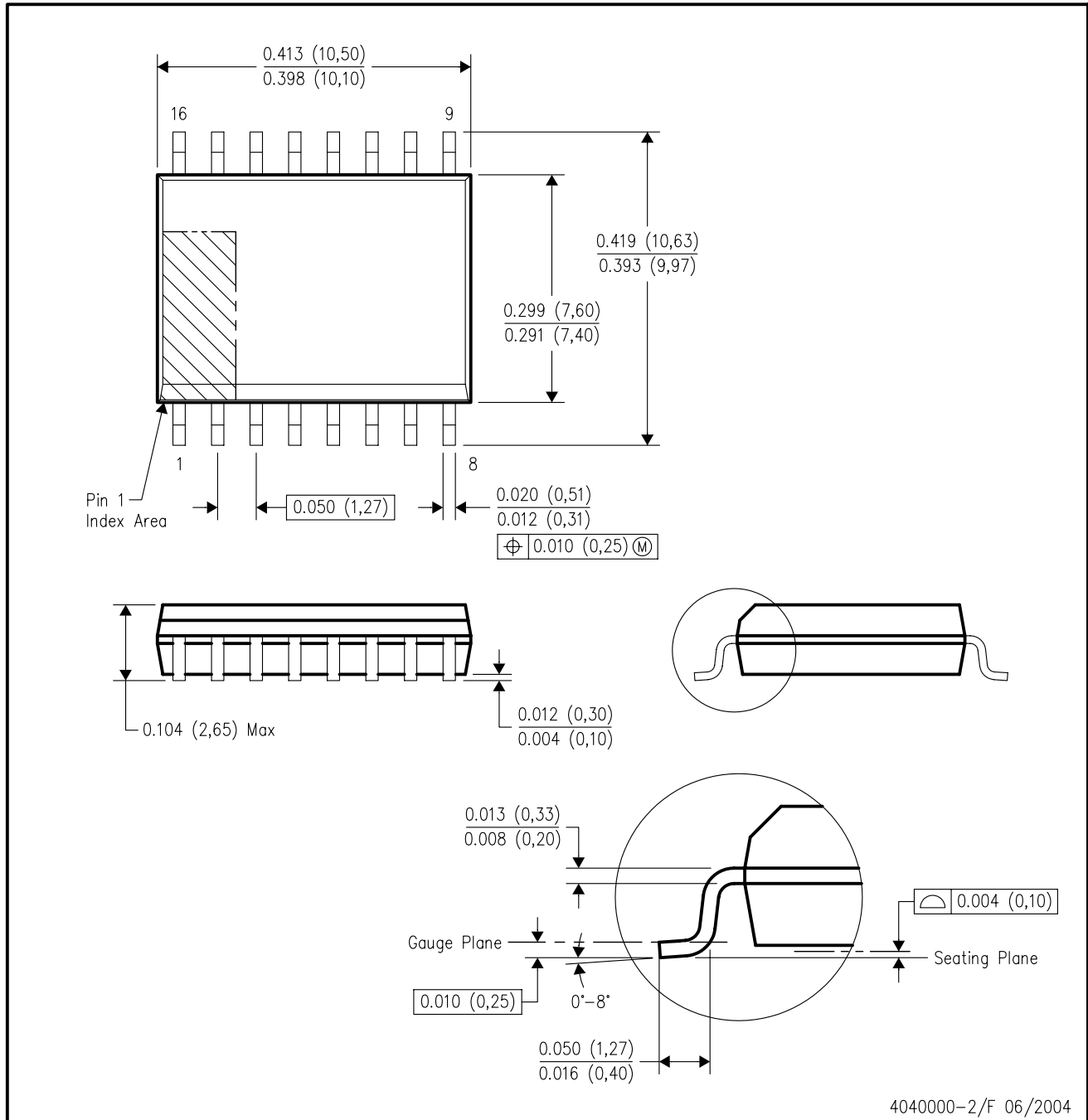
TAPE AND REEL BOX DIMENSIONS



Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
ISO7240ADWR	DW	16	SITE 35	406.0	348.0	63.0
ISO7240CDWR	DW	16	SITE 35	406.0	348.0	63.0
ISO7240MDWR	DW	16	SITE 35	406.0	348.0	63.0
ISO7241ADWR	DW	16	SITE 35	406.0	348.0	63.0
ISO7241CDWR	DW	16	SITE 35	406.0	348.0	63.0
ISO7241MDWR	DW	16	SITE 35	406.0	348.0	63.0
ISO7242ADWR	DW	16	SITE 35	406.0	348.0	63.0
ISO7242CDWR	DW	16	SITE 35	406.0	348.0	63.0
ISO7242MDWR	DW	16	SITE 35	406.0	348.0	63.0

DW (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE



4040000-2/F 06/2004

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-013 variation AA.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		Applications	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
RFID	www.ti-rfid.com	Telephony	www.ti.com/telephony
Low Power Wireless	www.ti.com/lpw	Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2007, Texas Instruments Incorporated