DUAL DIGITAL ISOLATORS

Check for Samples: ISO7220A-Q1, ISO7221A-Q1, ISO7221C-Q1

FEATURES

- **Qualified for Automotive Applications**
- **1-Mbps and 25-Mbps Signaling Rate Options**
  - **Low Channel-to-Channel Output Skew: 1 ns (Max)**
  - **Low Pulse-Width Distortion (PWD): 1 ns (Max)**
  - **Low Jitter Content: 1 ns (Typ) at 150 Mbps**
- **25-Year (Typ) Life at Rated Voltage (See Application Report SLLA197 and Figure 14)**
- **4000-V_{peak} Isolation, 560 V_{peak} V_{IORM}**
  - **UL 1577, IEC 60747-5-2 (VDE 0884, Rev 2), IEC 61010-1, IEC 60950-1 and CSA Approved**
  - **50 kV/μs Typical Transient Immunity**
- **Operates with 3.3-V or 5-V Supplies**
- **4 kV ESD Protection**
- **High Electromagnetic Immunity**
- **–40°C to 125°C Operating Free-Air Temperature Range**

DESCRIPTION

The ISO7220 and ISO7221 are dual-channel digital isolators. To facilitate PCB layout, the channels are oriented in the same direction in the ISO7220 and in opposite directions in the ISO7221. These devices have a logic input and output buffer separated by TI's silicon-dioxide (SiO_2) isolation barrier, providing galvanic isolation of up to 4000 V. Used in conjunction with isolated power supplies, these devices block high voltage, isolate grounds, and prevent noise currents on a data bus or other circuits from entering the local ground and interfering with or damaging sensitive circuitry.

A binary input signal is conditioned, translated to a balanced signal, then differentiated by the capacitive isolation barrier. Across the isolation barrier, a differential comparator receives the logic transition information, then sets or resets a flip-flop and the output circuit accordingly. A periodic update pulse is sent across the barrier to ensure the proper dc level of the output. If this dc-refresh pulse is not received every 4 μs, the input is assumed to be unpowered or not being actively driven, and the failsafe circuit drives the output to a logic high state.

The small capacitance and resulting time constant provide fast operation with signaling rates available from 0 Mbps (dc) to 25 Mbps.(1)The A-option and C-option devices have TTL input thresholds and a noise filter at the input that prevents transient pulses from being passed to the output of the device.

These devices require two supply voltages of 3.3 V, 5 V, or any combination. All inputs are 5-V tolerant when supplied from a 3.3-V supply and all outputs are 4-mA CMOS.

These devices are characterized for operation over the ambient temperature range of –40°C to 125°C.

(1) The signaling rate of a line is the number of voltage transitions that are made per second expressed in the units bps (bits per second).

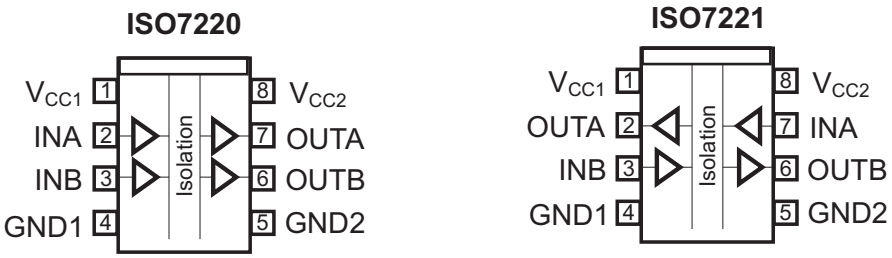
This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

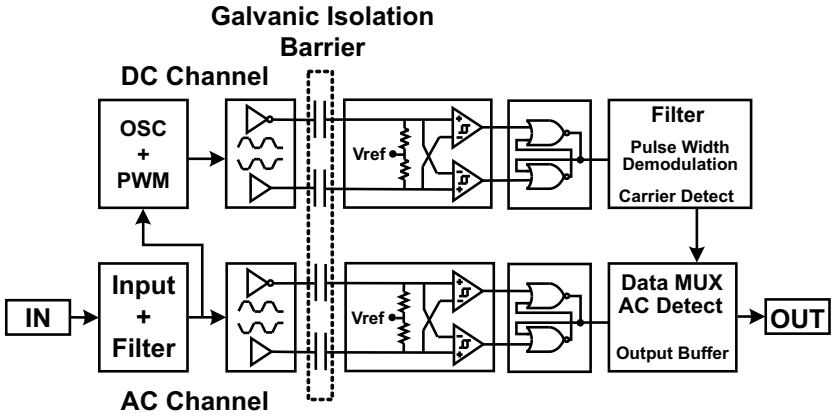
ORDERING INFORMATION(1)

T_A	SIGNALING RATE	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	1 Mbps	SOIC – D	Reel of 2500	ISO7220AQDRQ1	7220AQ
	1 Mbps	SOIC – D	Reel of 2500	ISO7221AQDRQ1	7221AQ
	25 Mbps	SOIC – D	Reel of 2500	ISO7221CQDRQ1	7221CQ

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.



SINGLE-CHANNEL FUNCTION DIAGRAM



REGULATORY INFORMATION

VDE	CSA	UL
Certified according to IEC 60747-5-2	Approved under CSA Component Acceptance Notice	Recognized under 1577 Component Recognition Program(1)
File Number: 40016131	File Number: 1698195	File Number: E181974

(1) Production tested ≥3000 VRMS for 1 second in accordance with UL 1577.

ABSOLUTE MAXIMUM RATINGS(1)

V_{CC}	Supply voltage(2), V_{CC1}, V_{CC2}			–0.5 V to 6 V
V_I	Voltage at IN, OUT			–0.5 V to 6 V
I_O	Output current			±15 mA
ESD	Electrostatic discharge	Human-Body Model	All pins	±4 kV
		Field-Induced Charged-Device Model		±1 kV
		Machine Model		±200 V
T_J	Maximum junction temperature			150°C
T_{stg}	Storage temperature			–65°C to 150°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values except differential I/O bus voltages are with respect to network ground terminal and are peak voltage values.

RECOMMENDED OPERATING CONDITIONS

			MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage(1)	V_{CC1}, V_{CC2}	3		5.5	V
I_{OH}	High-level output current				4	mA
I_{OL}	Low-level output current		–4			mA
t_{ui}	Input pulse width	ISO722xA	1	0.67		µs
		ISO722xC	40	33		ns
$1/t_{ui}$	Signaling rate	ISO722xA	0	1500	1000	kbps
		ISO722xC	0	30	25	Mbps
V_{IH}	High-level input voltage		2		V_{CC}	V
V_{IL}	Low-level input voltage		0		0.8	V
T_J	Operating virtual-junction temperature		–40		150	°C
H	External magnetic field-strength immunity per IEC 61000-4-8 and IEC 61000-4-9 certification				1000	A/m

(1) For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V.
For the 3-V operation, V_{CC1} or V_{CC2} is specified from 3 V to 3.6 V.

ELECTRICAL CHARACTERISTICS

V_{CC1} and V_{CC2} at 5 V[1], over recommended operating conditions (unless otherwise noted)

PARAMETER				TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC1}	Supply current, V_{CC1}	ISO7220x	Quiescent	V_I = V_{CC} or 0 V, no load		1	2	mA
		ISO7221x				8.5	17	
		ISO7220A	1 Mbps			2	3	
		ISO7221A				10	18	
		ISO7221C	25 Mbps			12	22	
I_{CC2}	Supply current, V_{CC2}	ISO7220x	Quiescent	V_I = V_{CC} or 0 V, no load		16	31	mA
		ISO7221x				8.5	17	
		ISO7220A	1 Mbps			17	32	
		ISO7221A				10	18	
		ISO7221C	25 Mbps			12	22	
V_{OH}	High-level output voltage			I_{OH} = –4 mA, See Figure 1	V_{CC} – 0.8	4.6		V
				I_{OH} = –20 µA, See Figure 1	V_{CC} – 0.1	5		
V_{OL}	Low-level output voltage			I_{OL} = 4 mA, See Figure 1		0.2	0.4	V
				I_{OL} = 20 µA, See Figure 1		0	0.1	
$V_{I(HYS)}$	Input voltage hysteresis					150		mV
I_{IH}	High-level input current			IN from 0 V to V_{CC}			10	µA
I_{IL}	Low-level input current			IN from 0 V to V_{CC}	–10			µA
C_I	Input capacitance to ground			IN at V_{CC}, V_I = 0.4 sin (4E6πt)		1		pF
CMTI	Common-mode transient immunity			V_I = V_{CC} or 0 V, See Figure 3	25	50		kV/µs

(1) For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V.
For the 3-V operation, V_{CC1} or V_{CC2} is specified from 3 V to 3.6 V.

SWITCHING CHARACTERISTICS

V_{CC1} = V_{CC2} = 5 V, over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pLH}, t_{pHL}	Propagation delay	ISO722xA	See Figure 1	280	405	480	ns
PWD	Pulse-width distortion $\lvert t_{pHL} - t_{pLH} \rvert$ [1]				1	14	ns
t_{pLH}, t_{pHL}	Propagation delay	ISO722xC	See Figure 1	22	32	42	ns
PWD	Pulse-width distortion $\lvert t_{pHL} - t_{pLH} \rvert$ [1]				1	2	ns
$t_{sk(pp)}$	Part-to-part skew [2]	ISO722xA				180	ns
		ISO722xC				10	
$t_{sk(o)}$	Channel-to-channel output skew [3]	ISO722xA			3	15	ns
		ISO722xC			0.2	1	
t_r	Output signal rise time		See Figure 1		1		ns
t_f	Output signal fall time		See Figure 1		1		ns
t_{fs}	Failsafe output delay time from input power loss		See Figure 2		3		µs

(1) Also referred to as pulse skew.
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
(3) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

ELECTRICAL CHARACTERISTICS

V_{CC1} = 5 V, V_{CC2} = 3.3 V(1), over recommended operating conditions (unless otherwise noted)

PARAMETER				TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC1}	Supply current, V_{CC1}	ISO7220x	Quiescent	V_I = V_{CC} or 0 V, no load		1	2	mA
		ISO7221x				8.5	17	
		ISO7220A	1 Mbps	V_I = V_{CC} or 0 V, no load		2	3	
		ISO7221A				10	18	
		ISO7221C	25 Mbps	V_I = V_{CC} or 0 V, no load		12	22	
I_{CC2}	Supply current, V_{CC2}	ISO7220x	Quiescent	V_I = V_{CC} or 0 V, no load		8	18	mA
		ISO7221x				4.3	9.5	
		ISO7220A	1 Mbps	V_I = V_{CC} or 0 V, no load		9	19	
		ISO7221A				5	11	
		ISO7221C	25 Mbps	V_I = V_{CC} or 0 V, no load		6	12	
V_{OH}	High-level output voltage		ISO7220x	I_{OH} = –4 mA, See Figure 1	V_{CC} – 0.4			V
			ISO7221x (5-V side)		V_{CC} – 0.8			
				I_{OH} = –20 µA, See Figure 1	V_{CC} – 0.1			
V_{OL}	Low-level output voltage			I_{OL} = 4 mA, See Figure 1			0.4	V
				I_{OL} = 20 µA, See Figure 1			0.1	
$V_{I(HYS)}$	Input voltage hysteresis					150		mV
I_{IH}	High-level input current			IN from 0 V to V_{CC}			10	µA
I_{IL}	Low-level input current			IN from 0 V to V_{CC}	–10			µA
C_I	Input capacitance to ground			IN at V_{CC}, V_I = 0.4 sin (4E6πt)		1		pF
CMTI	Common-mode transient immunity			V_I = V_{CC} or 0 V, See Figure 3	15	40		kV/µs

(1) For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V.
For the 3-V operation, V_{CC1} or V_{CC2} is specified from 3 V to 3.6 V.

SWITCHING CHARACTERISTICS

V_{CC1} = 5 V, V_{CC2} = 3.3 V, over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pLH}, t_{pHL}	Propagation delay	ISO722xA	See Figure 1	285	410	480	ns
PWD	Pulse-width distortion $\lvert t_{pHL} - t_{pLH} \rvert$ (1)				1	14	ns
t_{pLH}, t_{pHL}	Propagation delay	ISO722xC	See Figure 1	25	36	48	ns
PWD	Pulse-width distortion $\lvert t_{pHL} - t_{pLH} \rvert$ (1)				1	2	ns
$t_{sk(pp)}$	Part-to-part skew (2)	ISO722xA				180	ns
		ISO722xC				10	
$t_{sk(o)}$	Channel-to-channel output skew (3)	ISO722xA			3	15	ns
		ISO722xC			0.2	1	
t_r	Output signal rise time		See Figure 1		2		ns
t_f	Output signal fall time		See Figure 1		2		
t_{fs}	Failsafe output delay time from input power loss		See Figure 2		3		µs

(1) Also referred to as pulse skew.
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
(3) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

ELECTRICAL CHARACTERISTICS

V_{CC1} = 3.3 V, V_{CC2} = 5 V[1], over recommended operating conditions (unless otherwise noted)

PARAMETER				TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC1}	Supply current, V_{CC1}	ISO7220x	Quiescent	V_I = V_{CC} or 0 V, no load		0.6	1	mA
		ISO7221x				4.3	9.5	
		ISO7220A	1 Mbps			1	2	
		ISO7221A				5	11	
		ISO7221C	25 Mbps			6	12	
I_{CC2}	Supply current, V_{CC2}	ISO7220x	Quiescent	V_I = V_{CC} or 0 V, no load		16	31	mA
		ISO7221x				8.5	17	
		ISO7220A	1 Mbps			18	32	
		ISO7221A				10	18	
		ISO7221C	25 Mbps			12	22	
V_{OH}	High-level output voltage		ISO7220x	I_{OH} = –4 mA, See Figure 1	V_{CC} – 0.8			V
			ISO7221x (3.3-V side)		V_{CC} – 0.4			
				I_{OH} = –20 µA, See Figure 1	V_{CC} – 0.1			
V_{OL}	Low-level output voltage			IOL = 4 mA, See Figure 1			0.4	V
				IOL = 20 µA, See Figure 1		0	0.1	
$V_{I(HYS)}$	Input threshold voltage hysteresis					150		mV
I_{IH}	High-level input current			IN from 0 V or V_{CC}			10	µA
I_{IL}	Low-level input current			IN from 0 V or V_{CC}	–10			µA
C_I	Input capacitance to ground			IN at V_{CC}, V_I = 0.4 sin (4E6πt)		1		pF
CMTI	Common-mode transient immunity			V_I = V_{CC} or 0 V, See Figure 3	15	40		kV/µs

(1) For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V.
For the 3-V operation, V_{CC1} or V_{CC2} is specified from 3 V to 3.6 V.

SWITCHING CHARACTERISTICS

V_{CC1} = 3.3 V, V_{CC2} = 5 V, over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pLH}, t_{pHL}	Propagation delay	ISO722xA	See Figure 1	285	395	480	ns
PWD	Pulse-width distortion $\lvert t_{pHL} - t_{pLH} \rvert$ (1)				1	18	ns
t_{pLH}, t_{pHL}	Propagation delay	ISO722xC	See Figure 1	24	36	48	ns
PWD	Pulse-width distortion $\lvert t_{pHL} - t_{pLH} \rvert$ (1)				1	3	ns
$t_{sk(pp)}$	Part-to-part skew (2)	ISO722xA				190	ns
		ISO722xC				10	
$t_{sk(o)}$	Channel-to-channel output skew (3)	ISO722xA			3	15	ns
		ISO722xC			0.2	1	
t_r	Output signal rise time		See Figure 1		1		ns
t_f	Output signal fall time		See Figure 1		1		ns
t_{fs}	Failsafe output delay time from input power loss		See Figure 2		3		µs

(1) Also referred to as pulse skew.
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
(3) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

ELECTRICAL CHARACTERISTICS

V_{CC1} = V_{CC2} = 3.3 V[1], over recommended operating conditions (unless otherwise noted)

PARAMETER				TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC1}	Supply current, V_{CC1}	ISO7220x	Quiescent	V_I = V_{CC} or 0 V, no load		0.6	1	mA
		ISO7221x				4.3	9.5	
		ISO7220A	1 Mbps			1	2	
		ISO7221A				5	11	
		ISO7221C	25 Mbps			6	12	
I_{CC2}	Supply current, V_{CC2}	ISO7220x	Quiescent	V_I = V_{CC} or 0 V, no load		8	18	mA
		ISO7221x				4.3	9.5	
		ISO7220A	1 Mbps			9	19	
		ISO7221A				5	11	
		ISO7221C	25 Mbps			6	12	
V_{OH}	High-level output voltage			I_{OH} = –4 mA, See Figure 1	V_{CC} – 0.4	3		V
				I_{OH} = –20 µA, See Figure 1	V_{CC} – 0.1	3.3		
V_{OL}	Low-level output voltage			I_{OL} = 4 mA, See Figure 1		0.2	0.4	V
				I_{OL} = 20 µA, See Figure 1		0	0.1	
$V_{I(HYS)}$	Input voltage hysteresis					150		mV
I_{IH}	High-level input current			IN from 0 V or V_{CC}			10	µA
I_{IL}	Low-level input current			IN from 0 V or V_{CC}	–10			µA
C_I	Input capacitance to ground			IN at V_{CC}, V_I = 0.4 sin (4E6πt)		1		pF
CMTI	Common-mode transient immunity			V_I = V_{CC} or 0 V, See Figure 3	15	40		kV/µs

(1) For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V.
For the 3-V operation, V_{CC1} or V_{CC2} is specified from 3 V to 3.6 V.

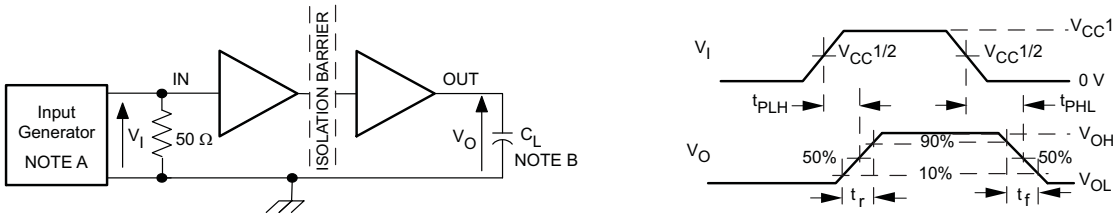
SWITCHING CHARACTERISTICS

V_{CC1} = V_{CC2} = 3.3 V, over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pLH}, t_{pHL}	Propagation delay	ISO722xA	See Figure 1	290	400	485	ns
PWD	Pulse-width distortion $\lvert t_{pHL} - t_{pLH} \rvert$[1]				1	18	ns
t_{pLH}, t_{pHL}	Propagation delay	ISO722xC	See Figure 1	25	40	52	ns
PWD	Pulse-width distortion $\lvert t_{pHL} - t_{pLH} \rvert$[1]				1	3	ns
$t_{sk(pp)}$	Part-to-part skew[2]	ISO722xA				190	ns
		ISO722xC				10	
$t_{sk(o)}$	Channel-to-channel output skew [3]	ISO722xA			3	15	ns
		ISO722xC			0.2	1	
t_r	Output signal rise time		See Figure 1		2		ns
t_f	Output signal fall time		See Figure 1		2		ns
t_{fs}	Failsafe output delay time from input power loss		See Figure 2		3		µs

(1) Also referred to as pulse skew.
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
(3) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

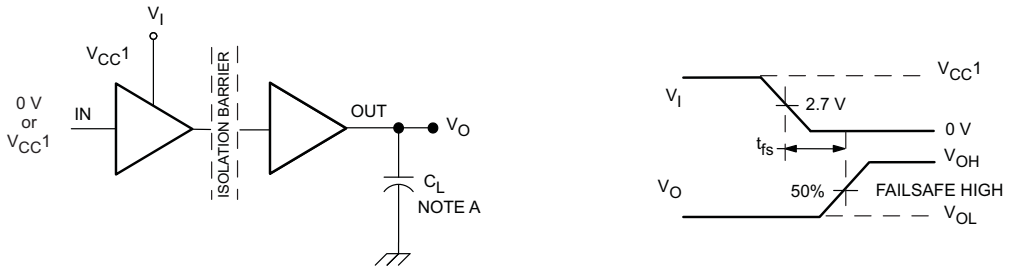
PARAMETER MEASUREMENT INFORMATION



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3 ns, Z_O = 50Ω.

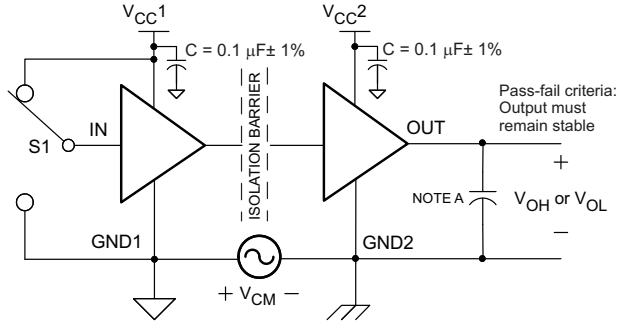
B. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 1. Switching Characteristic Test Circuit and Voltage Waveforms



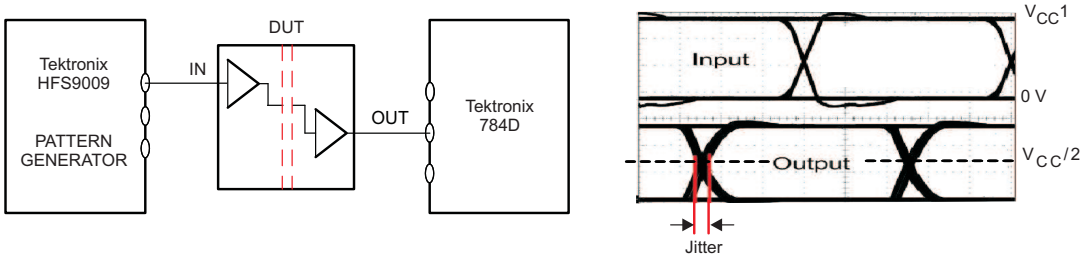
A. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 2. Failsafe Delay Time Test Circuit and Voltage Waveforms



A. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 3. Common-Mode Transient Immunity Test Circuit



NOTE: PRBS bit pattern run length is 2^{16} – 1. Transition time is 800 ps.

Figure 4. Peak-to-Peak Eye-Pattern Jitter Test Circuit and Voltage Waveform

DEVICE INFORMATION

IEC PACKAGE CHARACTERISTICS

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
L(I01)	Minimum air gap (clearance)	Shortest terminal-to-terminal distance through air	SOIC-8	4.8			mm
L(I02)	Minimum external tracking (creepage)	Shortest terminal-to-terminal distance across the package surface		4.3			mm
CTI	Tracking resistance (comparative tracking index)	DIN IEC 60112 / VDE 0303 Part 1		≥175			V
	Minimum internal gap (internal clearance)	Distance through the insulation		0.008			mm
R_{IO}	Isolation resistance	Input to output, V_{IO} = 500 V, all pins on each side of the barrier tied together creating a two-terminal device, T_A < 100°C			$>10^{12}$		Ω
		Input to output, V_{IO} = 500 V, 100°C ≤ T_A ≤ max			$>10^{11}$		Ω
C_{IO}	Barrier capacitance input to output	V_I = 0.4 sin (4E6πt)			1		pF
C_I	Input capacitance to ground	V_I = 0.4 sin (4E6πt)			1		pF

NOTE: Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed circuit board do not reduce this distance.

Creepage and clearance on a printed circuit board become equal according to the measurement techniques shown in the *Isolation Glossary* . Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.

IEC 60664-1 RATINGS TABLE

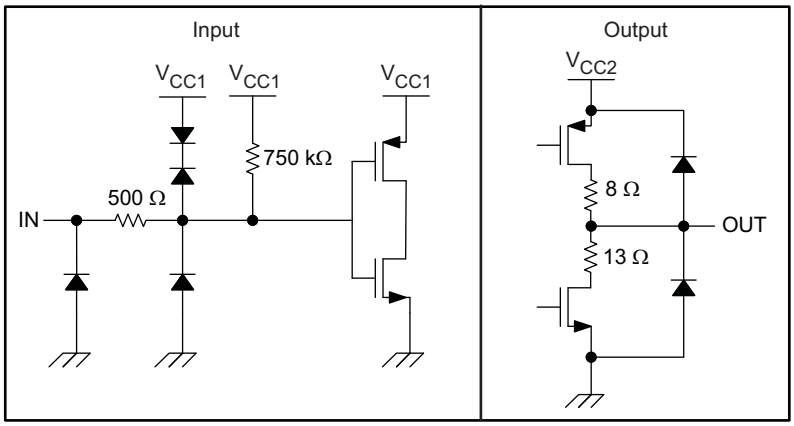
PARAMETER	TEST CONDITIONS	SPECIFICATION
Basic isolation group	Material group	IIIa
Installation classification	Rated mains voltage ≤150 VRMS	I-IV
	Rated mains voltage ≤300 VRMS	I-III
	Rated mains voltage ≤400 VRMS	I-II

IEC 60747-5-2 INSULATION CHARACTERISTICS(1)

PARAMETER		TEST CONDITIONS	SPECIFICATION	UNIT
V_{IORM}	Maximum working insulation voltage		560	V
V_{PR}	Input to output test voltage	Method b1, V_{PR} = V_{IORM} × 1.875, 100% Production test with t = 1 s, Partial discharge <5 pC	1050	V
V_{IOTM}	Transient overvoltage	t = 60 s	4000	V
R_S	Insulation resistance	V_{IO} = 500 V at T_S	$>10^9$	Ω
	Pollution degree		2	

(1) Climatic Classification 40/125/21

DEVICE I/O SCHEMATICS



IEC SAFETY LIMITING VALUES

Safety limiting intends to prevent potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the IO can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
I_S	Safety input, output, or supply current	SOIC-8	θ_{JA} = 212°C/W, V_I = 5.5 V, T_J = 170°C, T_A = 25°C		124	mA
			θ_{JA} = 212°C/W, V_I = 3.6 V, T_J = 170°C, T_A = 25°C		190	
T_S	Maximum case temperature	SOIC-8			150	°C

The safety-limiting constraint is the absolute maximum junction temperature specified in the absolute maximum ratings table. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in the Thermal Characteristics table is that of a device installed in the JESD51-3, Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages and is conservative. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

SOIC-8 PACKAGE THERMAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
θ_{JA}	Junction-to-air thermal resistance	Low-K thermal resistance(1)		212		°C/W
		High-K thermal resistance		122		
θ_{JB}	Junction-to-board thermal resistance			37		°C/W
θ_{JC}	Junction-to-case thermal resistance			69.1		°C/W

(1) Tested in accordance with the Low-K or High-K thermal metric definitions of EIA/JESD51-3 for leaded surface mount packages.

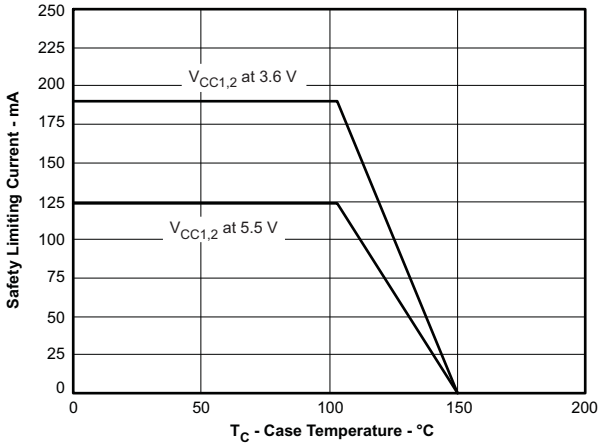


Figure 5. SOIC-8 θ_{JC} THERMAL DERATING CURVE per IEC 60747-5-2

DEVICE FUNCTION TABLE

Table 1. ISO7220x or ISO7221x(1)

INPUT SIDE V_{CC}	OUTPUT SIDE V_{CC}	INPUT IN	OUTPUT OUT
PU	PU	H	H
		L	L
		Open	H
PD	PU	X	H

(1) PU = Powered up(Vcc ≥ 3.0 V), PD = Powered down (Vcc ≤ 2.5 V), X = Irrelevant, H = High level, L = Low level

TYPICAL CHARACTERISTIC CURVES

3.3-V RMS SUPPLY CURRENT vs SIGNALING RATE (Mbps)

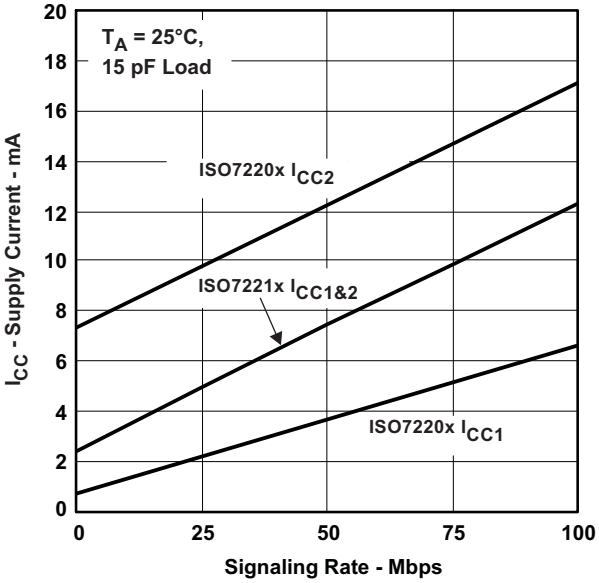


Figure 6.

5-V RMS SUPPLY CURRENT vs SIGNALING RATE (Mbps)

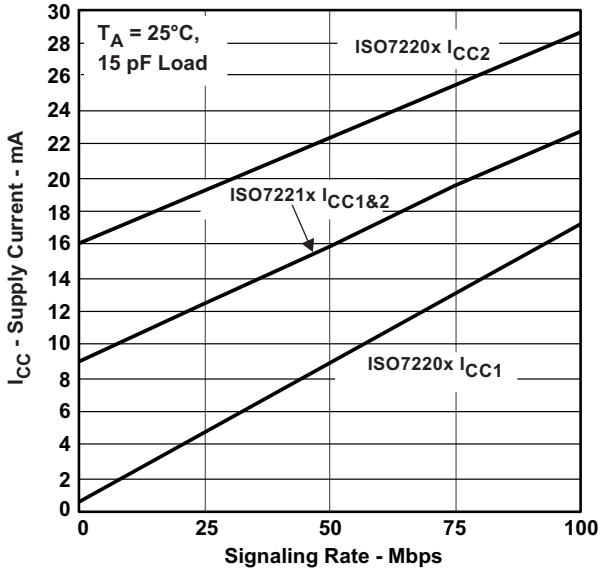


Figure 7.

ISO722xA AND ISO722xC INPUT VOLTAGE LOW-TO-HIGH SWITCHING THRESHOLD vs FREE-AIR TEMPERATURE

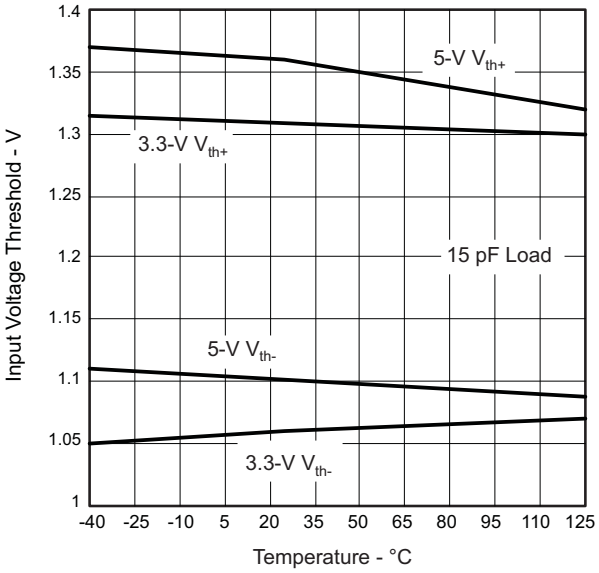


Figure 8.

V_{CC} FAILSAFE THRESHOLD vs FREE-AIR TEMPERATURE

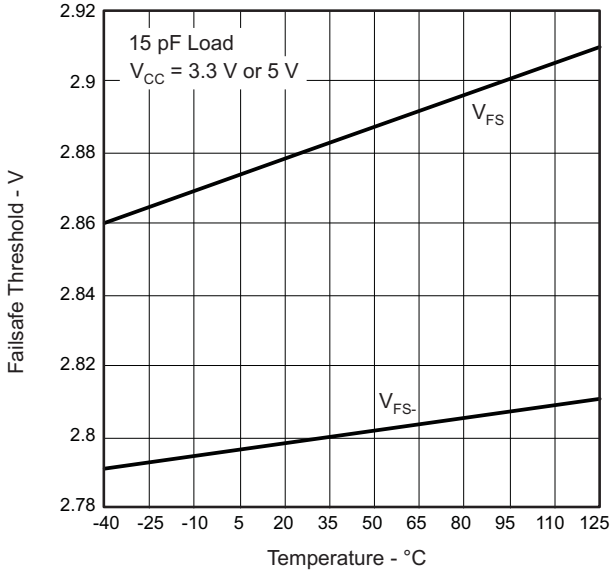


Figure 9.

TYPICAL CHARACTERISTIC CURVES (continued)

HIGH-LEVEL OUTPUT CURRENT vs HIGH-LEVEL OUTPUT VOLTAGE

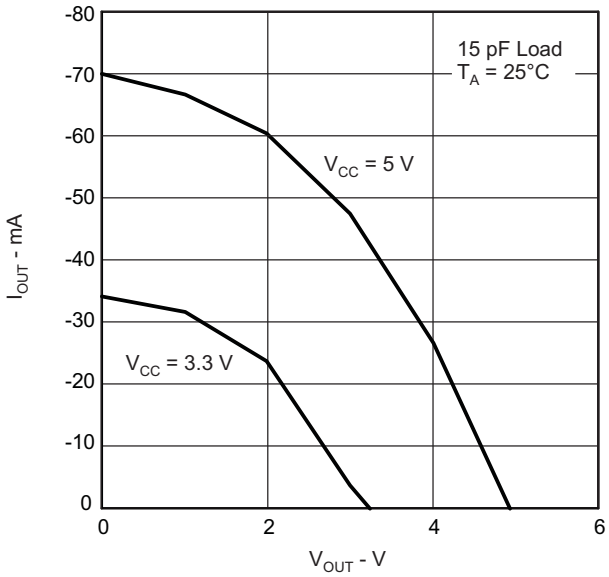


Figure 10.

LOW-LEVEL OUTPUT CURRENT vs LOW-LEVEL OUTPUT VOLTAGE

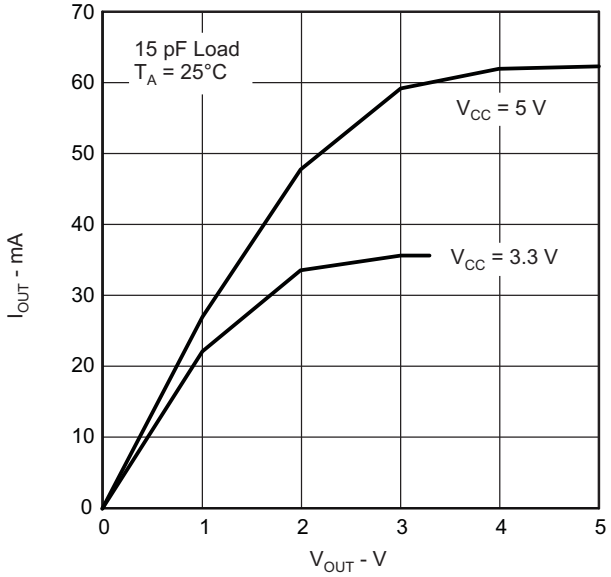


Figure 11.

APPLICATION INFORMATION

Typical Applications

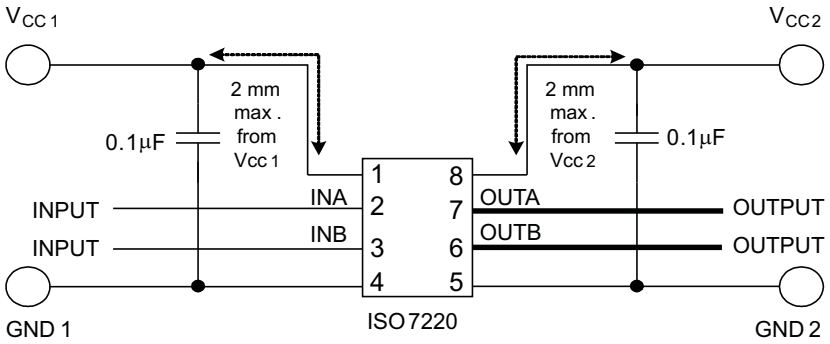


Figure 12. Typical ISO7220 Application Circuit

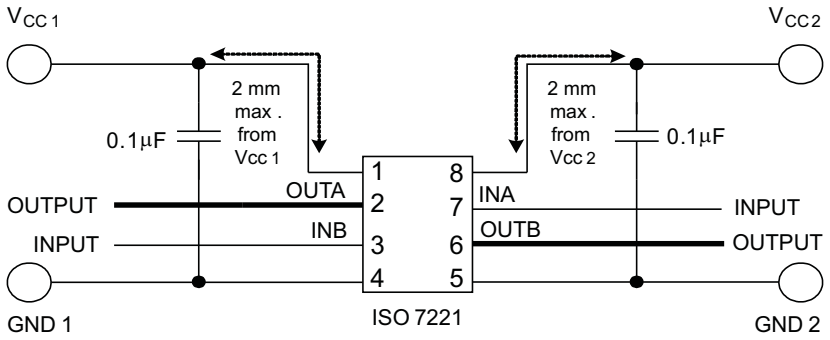


Figure 13. Typical ISO7221 Application Circuit

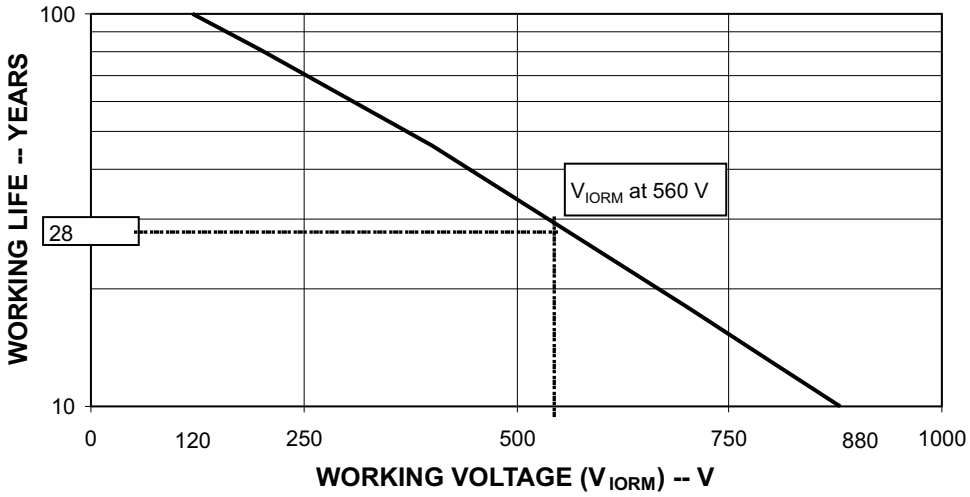
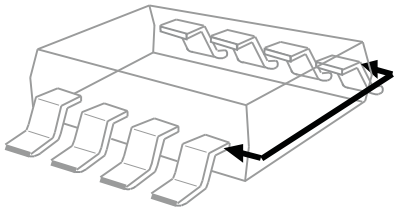


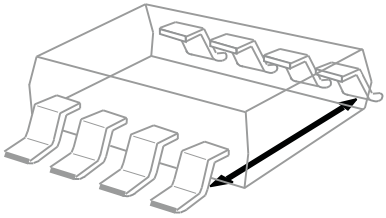
Figure 14. Time-Dependent Dielectric Breakdown Test Results

ISOLATION GLOSSARY

Creepage Distance — The shortest path between two conductive input to output leads measured along the surface of the insulation. The shortest distance path is found around the end of the package body.



Clearance — The shortest distance between two conductive input to output leads measured through air (line of sight).



Input-to Output Barrier Capacitance — The total capacitance between all input terminals connected together, and all output terminals connected together.

Input-to Output Barrier Resistance — The total resistance between all input terminals connected together, and all output terminals connected together.

Primary Circuit — An internal circuit directly connected to an external supply mains or other equivalent source which supplies the primary circuit electric power.

Secondary Circuit — A circuit with no direct connection to primary power, and derives its power from a separate isolated source.

Comparative Tracking Index (CTI) — CTI is an index used for electrical insulating materials which is defined as the numerical value of the voltage which causes failure by tracking during standard testing. Tracking is the process that produces a partially conducting path of localized deterioration on or through the surface of an insulating material as a result of the action of electric discharges on or close to an insulation surface -- the higher CTI value of the insulating material, the smaller the minimum creepage distance.

Generally, insulation breakdown occurs either through the material, over its surface, or both. Surface failure may arise from flashover or from the progressive degradation of the insulation surface by small localized sparks. Such sparks are the result of the breaking of a surface film of conducting contaminant on the insulation. The resulting break in the leakage current produces an overvoltage at the site of the discontinuity, and an electric spark is generated. These sparks often cause carbonization on insulation material and lead to a carbon track between points of different potential. This process is known as *tracking*.

Insulation:

Operational insulation — Insulation needed for the correct operation of the equipment.

Basic insulation — Insulation to provide basic protection against electric shock.

Supplementary insulation — Independent insulation applied in addition to basic insulation in order to ensure protection against electric shock in the event of a failure of the basic insulation.

Double insulation — Insulation comprising both basic and supplementary insulation.

Reinforced insulation — A single insulation system which provides a degree of protection against electric shock equivalent to double insulation.

Pollution Degree:

Pollution Degree 1 — No pollution, or only dry, nonconductive pollution occurs. The pollution has no influence.

Pollution Degree 2 — Normally, only nonconductive pollution occurs. However, a temporary conductivity caused by condensation must be expected.

Pollution Degree 3 — Conductive pollution occurs or dry nonconductive pollution occurs which becomes conductive due to condensation which is to be expected.

Pollution Degree 4 – Continuous conductivity occurs due to conductive dust, rain, or other wet conditions.

Installation Category:

Overvoltage Category — This section is directed at insulation co-ordination by identifying the transient overvoltages which may occur, and by assigning 4 different levels as indicated in IEC 60664.

I: Signal Level — Special equipment or parts of equipment.

II: Local Level — Portable equipment etc.

III: Distribution Level — Fixed installation

IV: Primary Supply Level — Overhead lines, cable systems

Each category should be subject to smaller transients than the category above.

REVISION HISTORY

Changes from Revision B (March 2010) to Revision C	Page
• Added storage temperature to Abs Max table.	3

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
ISO7220AQDRQ1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
ISO7221AQDRQ1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
ISO7221CQDRQ1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

OTHER QUALIFIED VERSIONS OF ISO7220A-Q1, ISO7221A-Q1, ISO7221C-Q1 :

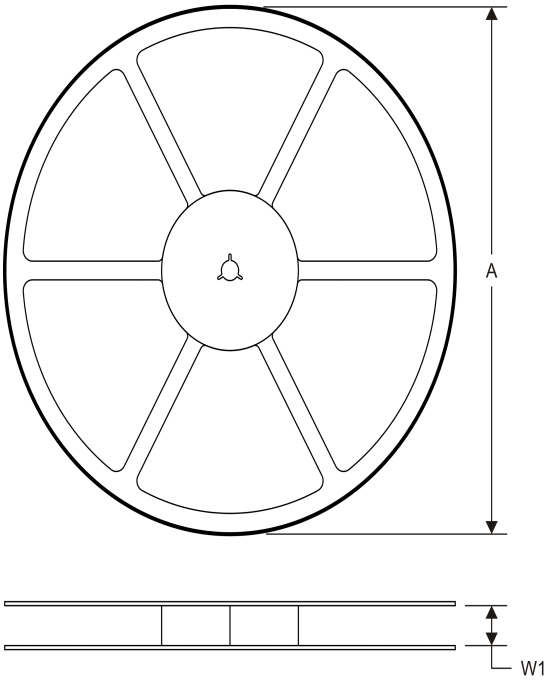
- Catalog: ISO7220A, ISO7221A, ISO7221C

NOTE: Qualified Version Definitions:

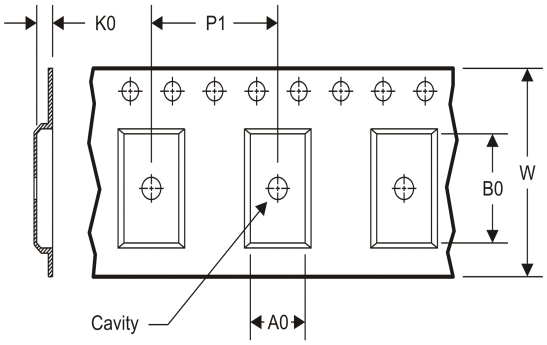
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



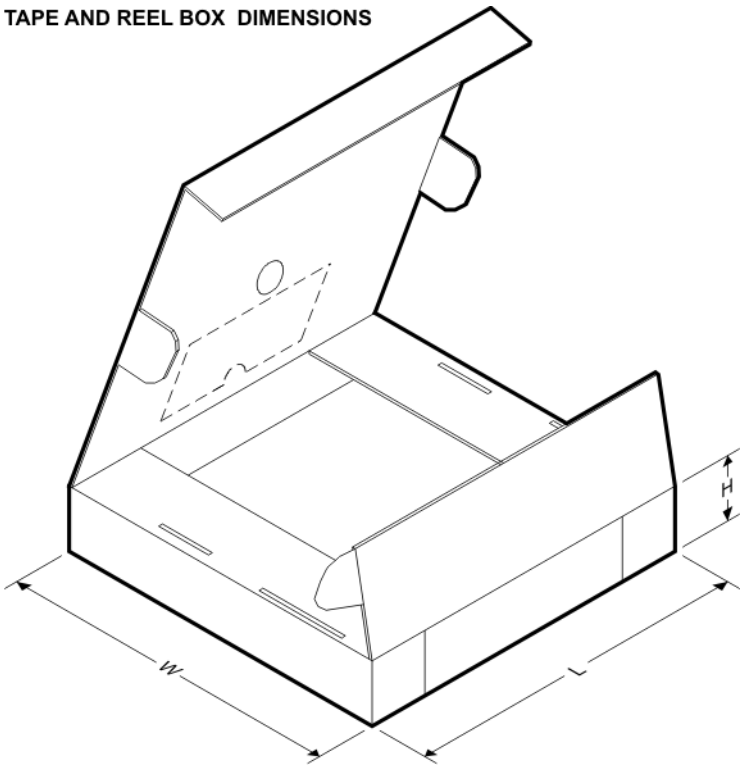
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO7220AQDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7221AQDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7221CQDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

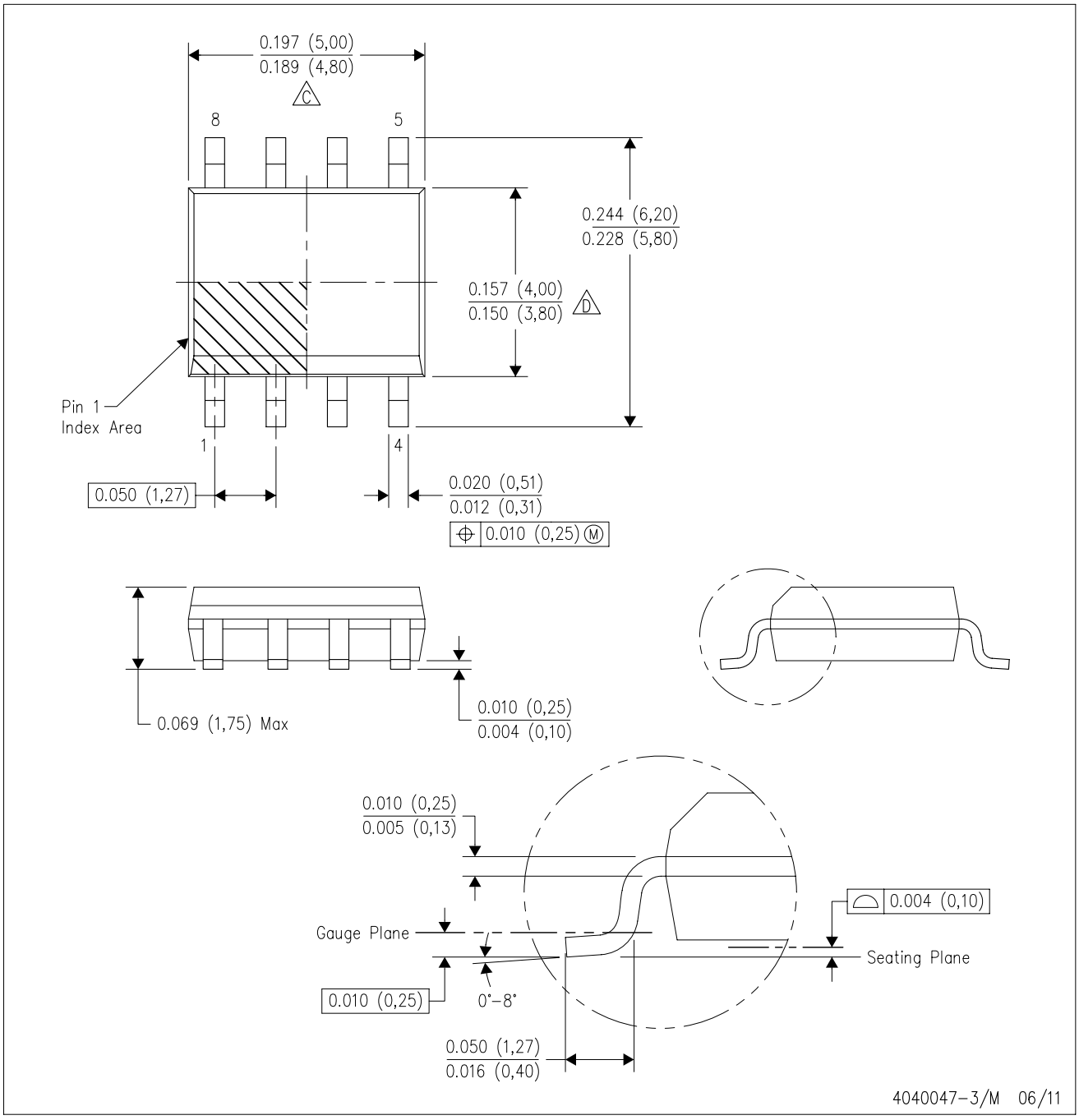
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

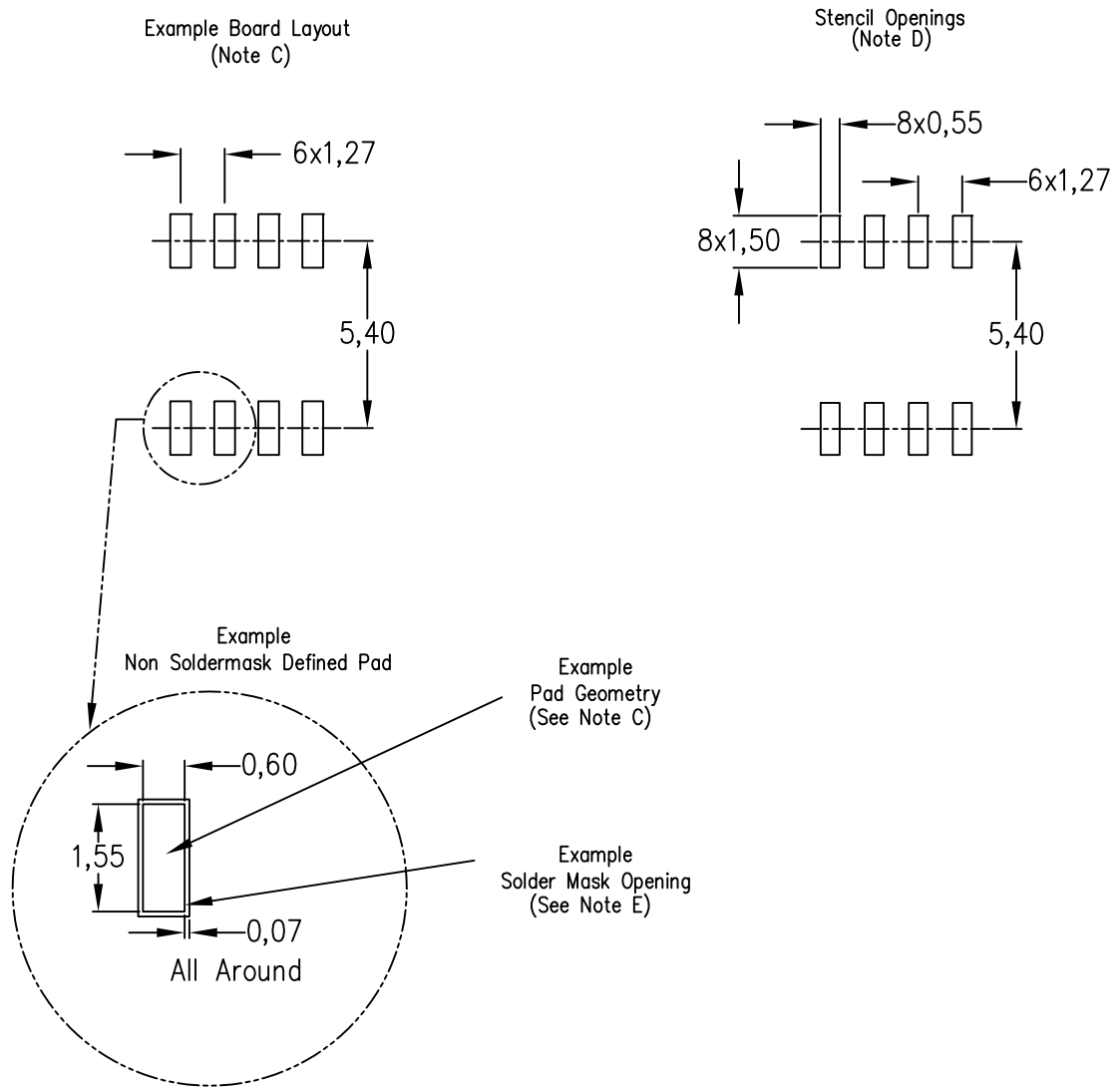
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO7220AQDRQ1	SOIC	D	8	2500	367.0	367.0	35.0
ISO7221AQDRQ1	SOIC	D	8	2500	367.0	367.0	35.0
ISO7221CQDRQ1	SOIC	D	8	2500	367.0	367.0	35.0

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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