I²C CONTROLLED KEYPAD SCAN IC WITH INTEGRATED ESD PROTECTION

FEATURES

- **Operating Power-Supply Voltage Range of 1.65 V to 3.6 V**
- **Supports QWERTY Keypad Operation Plus GPIO Expansion**
- **18 GPIOs Can Be Configured into Eight Inputs and Ten Outputs to Support an 8 × 10 Keypad Array (80 Buttons)**
- **ESD Protection Exceeds JESD 22 on all 18 GPIO Pins and non GPIO pins**
  - **2000-V Human Body Model (A114-A)**
  - **1000-V Charged Device Model (C101)**
- **Low Standby (Idle) Current Consumption: 3 μA**
- **Polling Current Drain 70 μA for One Key Pressed**
- **10 Byte FIFO to Store 10 Key Presses and Releases**
- **Supports 1-MHz Fast Mode Plus I²C Bus**
- **Open-Drain Active-Low Interrupt Output, Asserted when Key is Pressed and Key is Released**
- **Minimum Debounce Time of 50 μs**
- **Schmitt-Trigger Action Allows Slow Input Transition and Better Switching Noise Immunity at the SCL and SDA Inputs: Typical V_{hys} at 1.8 V is 0.18 V**
- **Latch-Up Performance Exceeds 200 mA Per JESD 78, Class II**
- **Very Small Packages**
  - **WCSP (YFP): 2 mm × 2 mm; 0.4 mm pitch**
  - **QFN (RTW): 4 mm × 4 mm; 0.5 mm pitch**

APPLICATIONS

- **Smart Phones**
- **PDAs**
- **GPS Devices**
- **MP3 Players**
- **Digital Cameras**

DESCRIPTION/ORDERING INFORMATION

The TCA8418 is a keypad scan device with integrated ESD protection. It can operate from 1.65 V to 3.6 V and has 18 general purpose inputs/outputs (GPIO) that can be used to support up to 80 keys via the I²C interface [serial clock (SCL), serial data (SDA)].

The key controller includes an oscillator that debounces at 50 μs and maintains a 10 byte FIFO of key-press and release events which can store up to 10 keys with overflow wrap capability. An interrupt (/INT) output can be configured to alert key presses and releases either as they occur, or at maximum rate. Also, for the YFP package, a CAD_INT pin is included to indicate the detection of CTRL-ALT-DEL (i.e., 1, 11, 21) key press action.

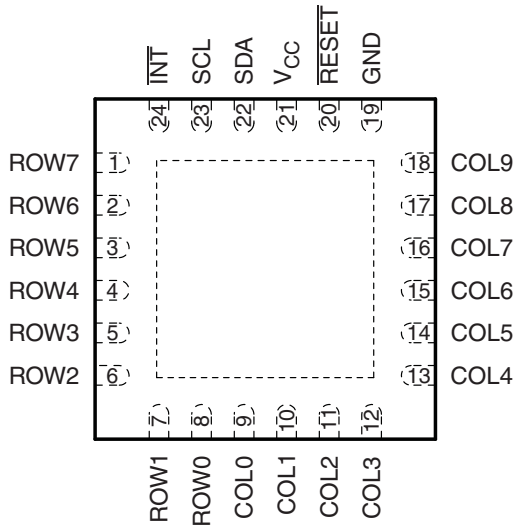
The major benefit of this device is it frees up the processor from having to scan the keypad for presses and releases. This provides power and bandwidth savings. The TCA8418 is also ideal for usage with processors that have limited GPIOs.

ORDERING INFORMATION

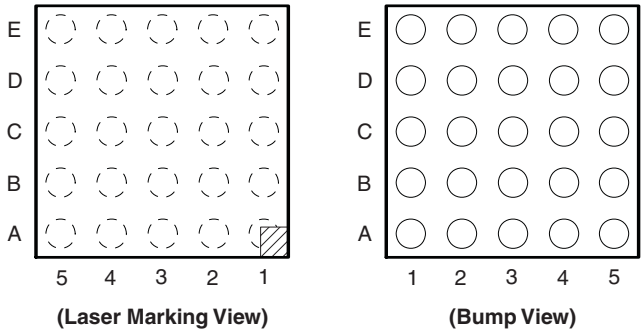
T_A	PACKAGE(1)(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	QFN – RTW	Tape and reel	TCA8418RTWR	PZ418
	WCSP – YFP	Tape and reel	TCA8418YFPR	PREVIEW

(1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

RTW PACKAGE
(TOP VIEW)



YFP PACKAGE



YFP Package Terminal Assignments

E	$\overline{INT}$	GND	COL5	COL0	ROW3
D	SCL	COL9	COL4	ROW0	ROW4
C	SDA	COL8	COL3	ROW1	ROW5
B	V_{CC}	COL7	COL2	$\overline{CAD\_INT}$	ROW6
A	$\overline{RESET}$	COL6	COL1	ROW2	ROW7
	5	4	**3**	**2**	**1**

TERMINAL FUNCTIONS

TERMINAL			TYPE	DESCRIPTION
NO.		NAME		
QFN (RTW)	WCSP (YFP)			
1	A1	ROW7	I/O	GPIO or row 7 in keypad matrix
2	B1	ROW6	I/O	GPIO or row 6 in keypad matrix
3	C1	ROW5	I/O	GPIO or row 5 in keypad matrix
4	D1	ROW4	I/O	GPIO or row 4 in keypad matrix
5	E1	ROW3	I/O	GPIO or row 3 in keypad matrix
6	A2	ROW2	I/O	GPIO or row 2 in keypad matrix
7	C2	ROW1	I/O	GPIO or row 1 in keypad matrix
8	D2	ROW0	I/O	GPIO or row 0 in keypad matrix
9	E2	COL0	I/O	GPIO or column 0 in keypad matrix
10	A3	COL1	I/O	GPIO or column 1 in keypad matrix
11	B3	COL2	I/O	GPIO or column 2 in keypad matrix
12	C3	COL3	I/O	GPIO or column 3 in keypad matrix
13	D3	COL4	I/O	GPIO or column 4 in keypad matrix
14	E3	COL5	I/O	GPIO or column 5 in keypad matrix
15	A4	COL6	I/O	GPIO or column 6 in keypad matrix
16	B4	COL7	I/O	GPIO or column 7 in keypad matrix
17	C4	COL8	I/O	GPIO or column 8 in keypad matrix
18	D4	COL9	I/O	GPIO or column 9 in keypad matrix
19	E4	GND	–	Ground
20	A5	$\overline{\text{RESET}}$	I	Active-low reset input. Connect to V_{CC} through a pullup resistor, if no active connection is used.
21	B5	V_{CC}	Pwr	Supply voltage of 1.65 V to 3.6 V
22	C5	SDA	I/O	Serial data bus. Connect to V_{CC} through a pullup resistor.
23	D5	SCL	I	Serial clock bus. Connect to V_{CC} through a pullup resistor.
24	E5	$\overline{\text{INT}}$	O	Active-low interrupt output. Open drain structure. Connect to V_{CC} through a pullup resistor.
–	B2	$\overline{\text{CAD\_INT}}$	O	Active-low interrupt hardware output for 3-key simultaneous press-event. Open drain structure. Connect to V_{CC} through a pullup resistor.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

				MIN	MAX	UNIT
V_{CC}	Supply voltage range			–0.5	4.6	V
V_I	Input voltage range(2)			–0.5	4.6	V
V_O	Voltage range applied to any output in the high-impedance or power-off state(2)			–0.5	4.6	V
	Output voltage range in the high or low state(2)			–0.5	4.6	
I_{IK}	Input clamp current	$V_I < 0$			±20	mA
I_{OK}	Output clamp current	$V_O < 0$			±20	mA
I_{OL}	Continuous output Low current	P port, SDA	V_O = 0 to V_{CC}		50	mA
		$\overline{INT}$			25	
I_{OH}	Continuous output High current	P port	V_O = 0 to V_{CC}		50	mA
T_{stg}	Storage temperature range			–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

THERMAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

				UNIT
θ_{JA}	Package thermal impedance(1)	RTW package	37.8	°C/W
		YFP package	TBD	

(1) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS

			MIN	MAX	UNIT
V_{CC}	Supply voltage		1.65	3.6	V
V_{IH}	High-level input voltage	SCL, SDA, ROW0–7, COL0–9, $\overline{RESET}$	0.7 × V_{CC}	3.6	V
V_{IL}	Low-level input voltage	SCL, SDA, ROW0–7, COL0–9, $\overline{RESET}$	–0.5	0.3 × V_{CC}	V
I_{OH}	High-level output current	ROW0–7, COL0–9		10	mA
I_{OL}	Low-level output current	ROW0–7, COL0–9		25	mA
T_A	Operating free-air temperature		–40	85	°C

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range, V_{CC} = 1.65 V to 3.6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS			V_{CCP}	MIN	TYP	MAX	UNIT
V_{IK}	Input diode clamp voltage	I_I = –18 mA			1.65 V to 3.6 V	–1.2			V
V_{POR}	Power-on reset voltage	$V_I = V_{CCP}$ or GND, I_O = 0			1.65 V to 3.6 V		1	1.4	V
V_{OH}	ROW0–7, COL0–9 high-level output voltage	I_{OH} = –1 mA			1.65 V	1.25			V
		I_{OH} = –8 mA			1.65 V	1.2			
					2.3 V	1.8			
					3 V	2.6			
		I_{OH} = –10 mA			1.65 V	1.1			
					2.3 V	1.7			
					3 V	2.5			
V_{OL}	ROW0–7, COL0–9 low-level output voltage	I_{OL} = 1 mA			1.65 V			0.4	V
		I_{OL} = 8 mA			1.65 V			0.45	
					2.3 V			0.25	
					3 V			0.25	
		I_{OL} = 10 mA			1.65 V			0.6	
					2.3 V			0.3	
					3 V			0.25	
I_{OL}	SDA	V_{OL} = 0.4 V			1.65 V to 3.6 V	3			mA
	$\overline{INT}$ and $\overline{CAD\_INT}$	V_{OL} = 0.4 V			1.65 V to 3.6 V	3			
I_I	SCL, SDA, ROW0–7, COL0–9, $\overline{RESET}$	$V_I = V_{CCI}$ or GND			1.65 V to 3.6 V			1	µA
r_{INT}	ROW0–7, COL0–9						105		kΩ
I_{CC}		V_I on SDA, ROW0–7, COL0–9 = V_{CC} or GND, I_O = 0, I/O = inputs,	f_{SCL} = 0 kHz	Oscillator OFF	1.65 V to 3.6 V			7	µA
				Oscillator ON				18	
			f_{SCL} = 400 kHz	1 key press	1.65 V			50	
					3.6 V			90	
			f_{SCL} = 1 MHz		1.65 V			65	
					3.6 V			153	
			f_{SCL} = 400 kHz	GPI low (pullup enable)(1)	1.65 V to 3.6 V			55	
			f_{SCL} = 1 MHz					65	
			f_{SCL} = 400 kHz	GPI low (pullup disable)				15	
			f_{SCL} = 1 MHz					24	
			f_{SCL} = 400 kHz	1 GPO active				55	
			f_{SCL} = 1 MHz					65	
C_I	SCL	$V_I = V_{CCI}$ or GND			1.65 V to 3.6 V		6	8	pF
C_{io}	SDA	$V_{IO} = V_{CC}$ or GND			1.65 V to 3.6 V		10	12.5	pF
	ROW0–7, COL0–9						5	6	

(1) Assumes that one GPIO is enabled.

I²C INTERFACE TIMING REQUIREMENTS

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 13)

		STANDARD MODE I²C BUS		FAST MODE I²C BUS		FAST MODE PLUS (FM+) I²C BUS		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f_{scl}	I²C clock frequency	0	100	0	400	0	1000	kHz
t_{sch}	I²C clock high time	4		0.6		0.26		µs
t_{scl}	I²C clock low time	4.7		1.3		0.5		µs
t_{sp}	I²C spike time		50		50		50	ns
t_{sds}	I²C serial data setup time	250		100		50		ns
t_{sdh}	I²C serial data hold time	0		0		0		ns
t_{icr}	I²C input rise time		1000	$20 + 0.1C_b$ (1)	300		120	ns
t_{icf}	I²C input fall time		300	$20 + 0.1C_b$ (1)	300		120	ns
t_{ocf}	I²C output fall time; 10 pF to 400 pF bus		300	$20 + 0.1C_b$ (1)	300		120	µs
t_{buf}	I²C bus free time between Stop and Start	4.7		1.3		0.5		µs
t_{sts}	I²C Start or repeater Start condition setup time	4.7		0.6		0.26		µs
t_{sth}	I²C Start or repeater Start condition hold time	4		0.6		0.26		µs
t_{sps}	I²C Stop condition setup time	4		0.6		0.26		µs
$t_{vd(data)}$	Valid data time; SCL low to SDA output valid		1		0.9		0.45	µs
$t_{vd(ack)}$	Valid data time of ACK condition; ACK signal from SCL low to SDA (out) low		1		0.9		0.45	µs

(1) C_b = total capacitance of one bus line in pF

RESET TIMING REQUIREMENTS

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 16)

		STANDARD MODE, FAST MODE, FAST MODE PLUS (FM+) I²C BUS		UNIT
		MIN	MAX	
t_W	Reset pulse duration	120 (1)		µs
t_{REC}	Reset recovery time	120 (1)		µs
t_{RESET}	Time to reset	120 (1)		µs

(1) The GPIO debounce circuit uses each GPIO input which passes through a two-stage register circuit. Both registers are clocked by the same clock signal, presumably free-running, with a nominal period of 50uS. When an input changes state, the new state is clocked into the first stage on one clock transition. On the next same-direction transition, if the input state is still the same as the previously clocked state, the signal is clocked into the second stage, and then on to the remaining circuits. Since the inputs are asynchronous to the clock, it will take anywhere from zero to 50 µsec after the input transition to clock the signal into the first stage. Therefore, the total debounce time may be as long as 100 µsec. Finally, to account for a slow clock, the spec further guard-banded at 120 µsec.

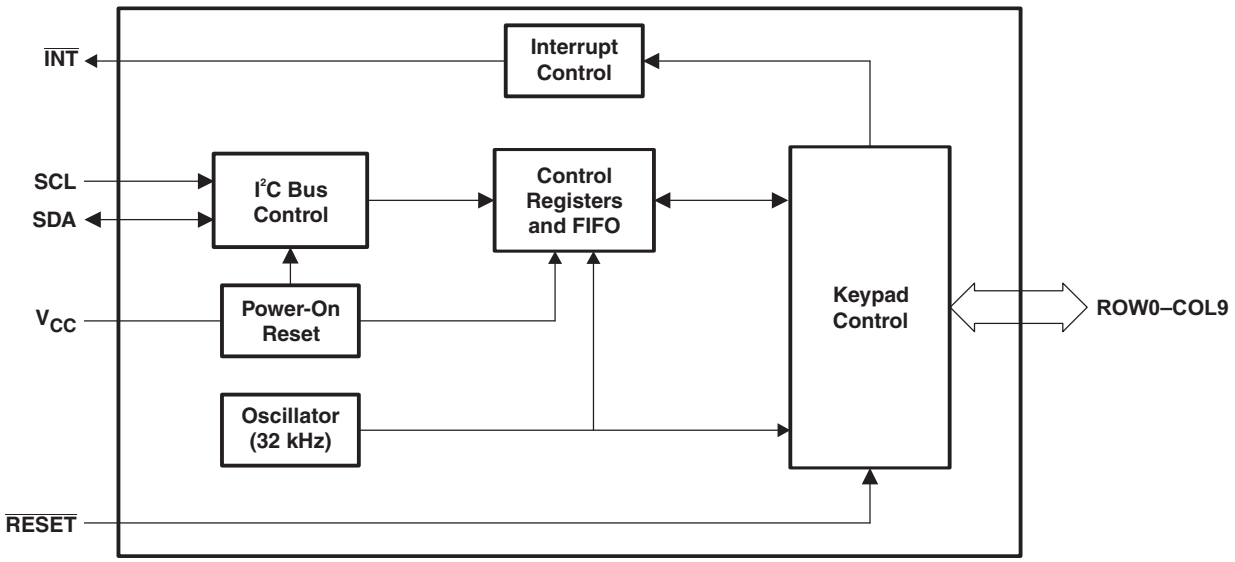
SWITCHING CHARACTERISTICS

PARAMETER			FROM	TO	STANDARD MODE, FAST MODE, FAST MODE PLUS (FM+) I^2C BUS		UNIT
					MIN	MAX	
t_{IV}	Interrupt valid time	Key event or Key unlock or Overflow	ROW0–7, COL0–9	$\overline{INT}$	20	60	µs
		GPI_INT with Debounce_DIS_Low			40	120	
		GPI_INT with Debounce_DIS_High			10	30	
		$\overline{CAD\_INT}$		$\overline{INT}$, $\overline{CAD\_INT}$	20	60	
t_{IR}	Interrupt reset delay time		SCL	$\overline{INT}$		200	ns
			SCL	$\overline{CAD\_INT}$			
t_{PV}	Output data valid		SCL	ROW0–7, COL0–9		400	ns
t_{PS}	Input data setup time		P port	SCL	0		ns
t_{PH}	Input data hold time		P port	SCL	300		ns

KEYPAD SWITCHING CHARACTERISTICS

PARAMETER	STANDARD MODE, FAST MODE, FAST MODE PLUS (FM+) I^2C BUS		UNIT
	MIN	MAX	
Key press to detection delay		25	µs
Key release to detection delay		25	µs
Keypad unlock timer		7	s
Keypad interrupt mask timer		31	s
Debounce		60	ms

LOGIC DIAGRAM (POSITIVE LOGIC)



At power on, the GPIOs (ROW0–7 and COL0–9) are configured as inputs with internal 100-kΩ pullups enabled. However, the system master can enable the GPIOs to function as inputs, outputs or as part of the keypad matrix. GPIOs not used for keypad control can be used to support other control features in the application.

ROW7–ROW0 are configured as inputs in GPIO mode with a push-pull structure, at power-on. In keyscan mode, each has an open-drain structure with a 100-kΩ pullup resistor and is used as an input.

COL9–COL0 are configured as inputs in GPIO mode with a push-pull structure, at power on. In keyscan mode, each has an open-drain structure and is used as an output.

The system master can reset the TCA8418E in the event of a timeout or other improper operation by asserting a low in the /RESET input, while keeping the V_{CC} at its operating level.

A reset can be accomplished by holding the $\overline{\text{RESET}}$ pin low for a minimum of t_W. The TCA8418E registers and I^2C/SMBus state machine are changed to their default state once $\overline{\text{RESET}}$ is low (0). When $\overline{\text{RESET}}$ is high (1), the I/O levels at the P port can be changed externally or through the master. This input requires a pull-up resistor to VCC, if no active connection is used.

The power-on reset puts the registers in their default state and initializes the I^2C/SMBus state machine. The $\overline{\text{RESET}}$ pin causes the same reset/initialization to occur without depowering the part. The $\overline{\text{RESET}}$ pin can also be used as a shutdown pin, if the phone is closed.

The open-drain interrupt ($\overline{\text{INT}}$) output is used to indicate to the system master that an input state (GPI or ROWs) has changed. $\overline{\text{INT}}$ can be connected to the interrupt input of a microcontroller. By sending an interrupt signal on this line, the remote input can inform the microcontroller if there is incoming data on its ports without having to communicate via the I^2C bus. Thus, the TCA8418E can remain a simple slave device.

The TCA8418E has key lock capability, which can trigger an interrupt at key presses and releases, if selected

Power-On Reset

When power (from 0 V) is applied to V_{CC}, an internal power-on reset holds the TCA8418E in a reset condition until V_{CC} reaches V_{POR}. At that time, the reset condition is released, and the TCA8418E registers and I^2C/SMBus state machine initialize to their default states. After that, V_{CC} must be lowered below 0.2 V and back up to the operating voltage for a power-reset cycle.

Power-On Reset Requirements

In the event of a glitch or data corruption, TCA8418E can be reset to its default conditions by using the power-on reset feature. Power-on reset requires that the device go through a power cycle to be completely reset. This reset also happens when the device is powered on for the first time in an application.

The two types of power-on reset are shown in Figure 1 and Figure 2.

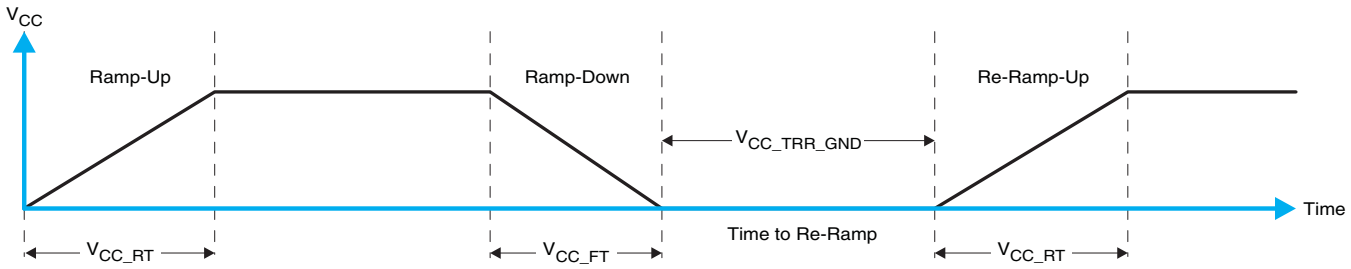


Figure 1. V_{CC} is Lowered Below 0.2 V or 0 V and Then Ramped Up to V_{CC}

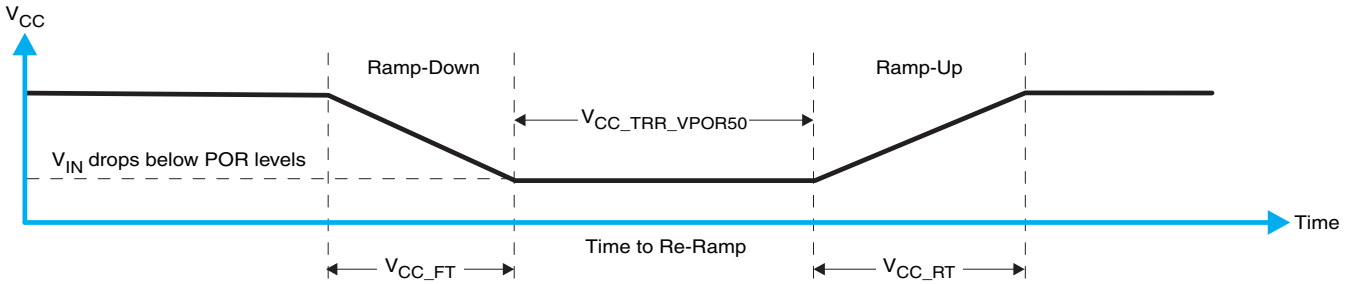


Figure 2. V_{CC} is Lowered Below the POR Threshold, Then Ramped Back Up to V_{CC}

Table 1 specifies the performance of the power-on reset feature for TCA8418E for both types of power-on reset.

Table 1. RECOMMENDED SUPPLY SEQUENCING AND RAMP RATES(1)

PARAMETER			MIN	TYP	MAX	UNIT
V_{CC_FT}	Fall rate	See Figure 1	1		100	ms
V_{CC_RT}	Rise rate	See Figure 1	0.01		100	ms
$V_{CC\_TRR\_GND}$	Time to re-ramp (when V_{CC} drops to GND)	See Figure 1	0.001			ms
$V_{CC\_TRR\_POR50}$	Time to re-ramp (when V_{CC} drops to V_{POR_MIN} – 50 mV)	See Figure 2	0.001			ms
V_{CC_GH}	Level that V_{CCP} can glitch down to, but not cause a functional disruption when V_{CCX_GW} = 1 µs	See Figure 3			1.2	V
V_{CC_GW}	Glitch width that will not cause a functional disruption when V_{CCX_GH} = 0.5 × V_{CCx}	See Figure 3				µs
V_{PORF}	Voltage trip point of POR on falling V_{CC}		0.767		1.144	V
V_{PORR}	Voltage trip point of POR on rising V_{CC}		1.033		1.428	V

(1) T_A = –40°C to 85°C (unless otherwise noted)

Glitches in the power supply can also affect the power-on reset performance of this device. The glitch width (V_{CC_GW}) and height (V_{CC_GH}) are dependent on each other. The bypass capacitance, source impedance, and device impedance are factors that affect power-on reset performance. Figure 3 and Table 1 provide more information on how to measure these specifications.

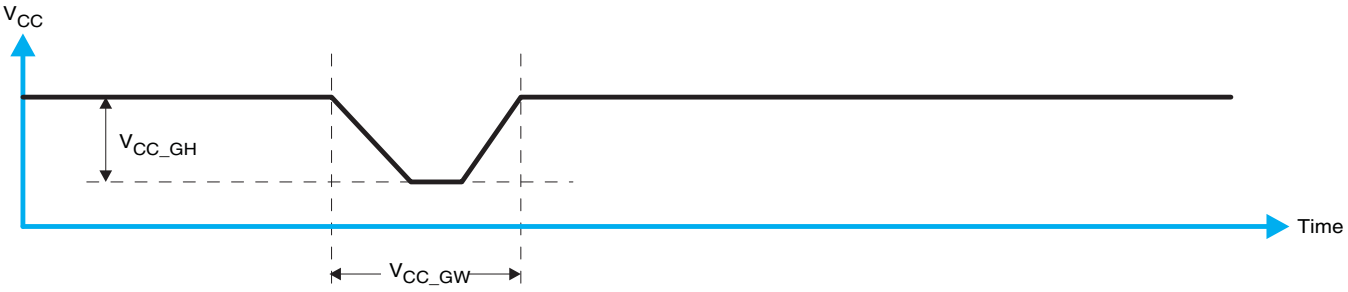


Figure 3. Glitch Width and Glitch Height

V_{POR} is critical to the power-on reset. V_{POR} is the voltage level at which the reset condition is released and all the registers and the I^2C/SMBus state machine are initialized to their default states. The value of V_{POR} differs based on the V_{CC} being lowered to or from 0. Figure 4 and Table 1 provide more details on this specification.

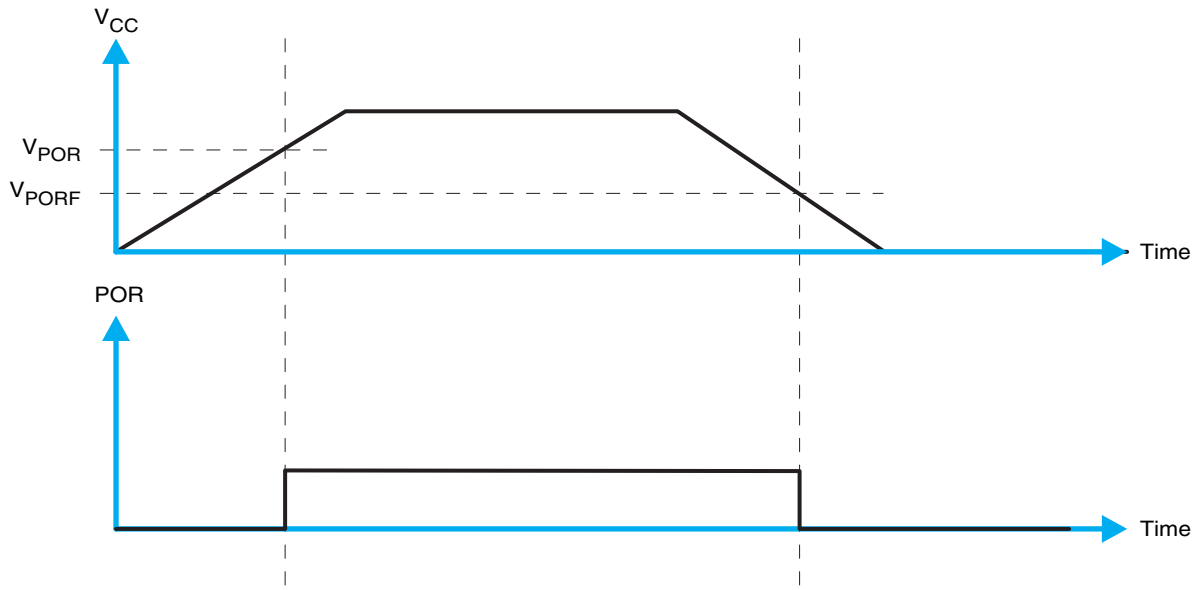


Figure 4. V_{POR}

For proper operation of the power-on reset feature, use as directed in the figures and table above.

Interrupt Output

An interrupt is generated by any rising or falling edge of the port inputs in the input mode. After time t_{iv}, the signal $\overline{INT}$ is valid. Resetting the interrupt circuit is achieved when data on the port is changed to the original setting or data is read from the port that generated the interrupt. Resetting occurs in the read mode at the acknowledge (ACK) or not acknowledge (NACK) bit after the rising edge of the SCL signal. Interrupts that occur during the ACK or NACK clock pulse can be lost (or be very short) due to the resetting of the interrupt during this pulse. Each change of the I/Os after resetting is detected and is transmitted as $\overline{INT}$.

Reading from or writing to another device does not affect the interrupt circuit, and a pin configured as an output cannot cause an interrupt. Changing an I/O from an output to an input may cause a false interrupt to occur, if the state of the pin does not match the contents of the input port register.

The $\overline{INT}$ output has an open-drain structure and requires a pullup resistor to V_{CC} depending on the application. If the $\overline{INT}$ signal is connected back to the processor that provides the SCL signal to the TCA64xxA, then the $\overline{INT}$ pin has to be connected to V_{CC}. If not, the $\overline{INT}$ pin can be connected to V_{CCP}.

For more information on the interrupt output feature, see Control Register and Command Byte and Typical Applications.

50 Micro-second Interrupt Configuration

The TCA8418 provides the capability of deasserting the interrupt for 50 µs while there is a pending event. When the INT_CFG bit in Register 0x01 is set, any attempt to clear the interrupt bit while the interrupt pin is already asserted results in a 50 µs deassertion. When the INT_CFG bit is cleared, processor interrupt remains asserted if the host tries to clear the interrupt. This feature is particularly useful for software development and edge triggering applications.

I^2C Interface

The bidirectional I^2C bus consists of the serial clock (SCL) and serial data (SDA) lines. Both lines must be connected to a positive supply through a pullup resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

I^2C communication with this device is initiated by a master sending a Start condition, a high-to-low transition on the SDA input/output, while the SCL input is high (see Figure 5). After the Start condition, the device address byte is sent, most significant bit (MSB) first, including the data direction bit (R/$\overline{W}$).

After receiving the valid address byte, this device responds with an acknowledge (ACK), a low on the SDA input/output during the high of the ACK-related clock pulse. The address (ADDR) input of the slave device must not be changed between the Start and the Stop conditions.

On the I^2C bus, only one data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high pulse of the clock period, as changes in the data line at this time are interpreted as control commands (Start or Stop) (see Figure 6).

A Stop condition, a low-to-high transition on the SDA input/output while the SCL input is high, is sent by the master (see Figure 5).

Any number of data bytes can be transferred from the transmitter to receiver between the Start and the Stop conditions. Each byte of eight bits is followed by one ACK bit. The transmitter must release the SDA line before the receiver can send an ACK bit. The device that acknowledges must pull down the SDA line during the ACK clock pulse, so that the SDA line is stable low during the high pulse of the ACK-related clock period (see Figure 7). When a slave receiver is addressed, it must generate an ACK after each byte is received. Similarly, the master must generate an ACK after each byte that it receives from the slave transmitter. Setup and hold times must be met to ensure proper operation.

A master receiver signals an end of data to the slave transmitter by not generating an acknowledge (NACK) after the last byte has been clocked out of the slave. This is done by the master receiver by holding the SDA line high. In this event, the transmitter must release the data line to enable the master to generate a Stop condition.

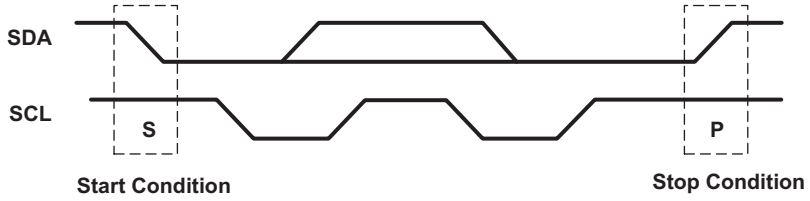


Figure 5. Definition of Start and Stop Conditions

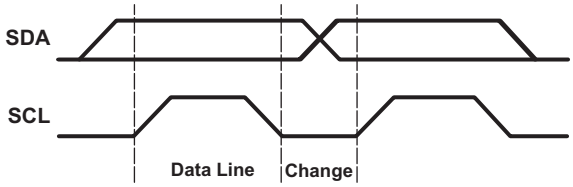


Figure 6. Bit Transfer

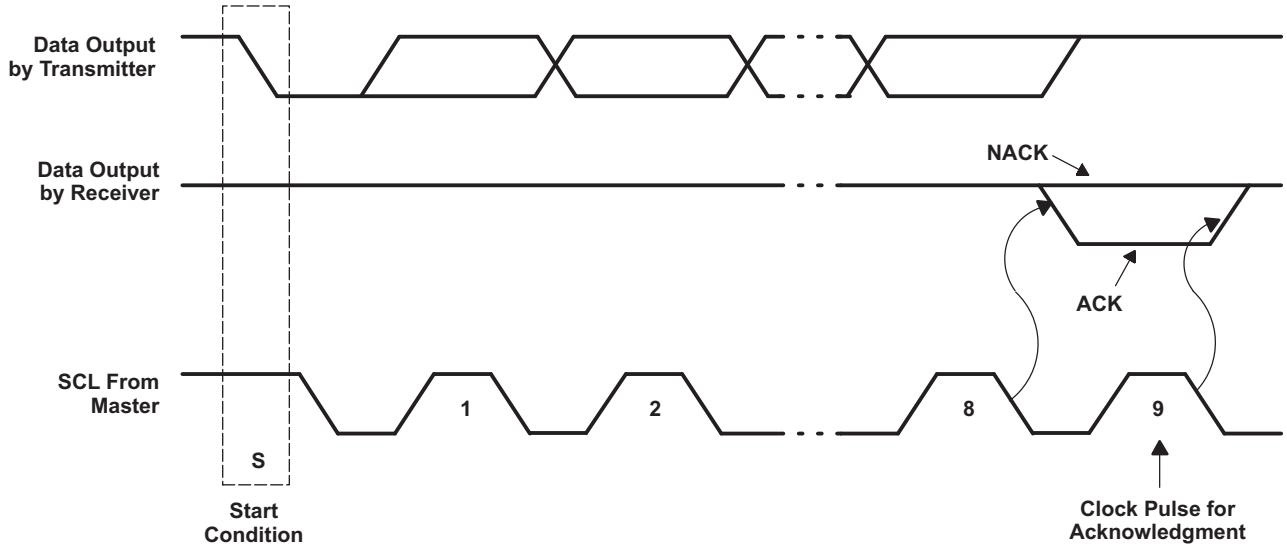


Figure 7. Acknowledgment on the I^2C Bus

Device Address

The address of the TCA8418E is shown in Table 2.

Table 2.

BYTE	BIT							
	7 (MSB)	6	5	4	3	2	1	0 (LSB)
I^2C slave address	0	1	1	0	1	0	0	R/$\overline{W}$

The last bit of the slave address defines the operation (read or write) to be performed. A high (1) selects a read operation, while a low (0) selects a write operation.

Control Register and Command Byte

Following the successful acknowledgment of the address byte, the bus master sends a command byte, which is stored in the control register in the TCA8418E. The command byte indicates the register that will be updated with information. All registers can be read and written to by the system master.

Table 3 shows all the registers within this device and their descriptions. The default value in all registers is 0.

Table 3. Register Descriptions

ADDRESS	REGISTER NAME	REGISTER DESCRIPTION	7	6	5	4	3	2	1	0
0×00	Reserved	Reserved								
0×01	CFG	Configuration register (interrupt processor interrupt enables)	AI	GPI_E_CGF	OVR_FLOW_M	INT_CFG	OVR_FLOW_IEN	K_LCK_IEN	GPI_IEN	KE_IEN
0×02	INT_STAT	Interrupt status register	N/A 0	N/A 0	N/A 0	N/A 0	OVR_FLOW_INT	K_LCK_INT	GPI_INT	K_ INT
0×03	KEY_LCK_EC	Key lock and event counter register	N/A 0	K_LCK_EN	LCK2	LCK1	KLEC3	KLEC2	KLEC1	KLEC0
0×04	KEY_EVENT_A	Key event register A	KEA7 0	KEA6 0	KEA5 0	KEA4 0	KEA3 0	KEA2 0	KEA1 0	KEA0 0
0×05	KEY_EVENT_B	Key event register B	KEB7 0	KEB6 0	KEB5 0	KEB4 0	KEB3 0	KEB2 0	KEB1 0	KEB0 0
0×06	KEY_EVENT_C	Key event register C	KEC7 0	KEC6 0	KEC5 0	KEC4 0	KEC3 0	KEC2 0	KEC1 0	KEC0 0
0×07	KEY_EVENT_D	Key event register D	KED7 0	KED6 0	KED5 0	KED4 0	KED3 0	KED2 0	KED1 0	KED0 0
0×08	KEY_EVENT_E	Key event register E	KEE7 0	KEE6 0	KEE5 0	KEE4 0	KEE3 0	KEE2 0	KEE1 0	KEE0 0
0×09	KEY_EVENT_F	Key event register F	KEF7 0	KEF6 0	KEF5 0	KEF4 0	KEF3 0	KEF2 0	KEF1 0	KEF0 0
0×0A	KEY_EVENT_G	Key event register G	KEG7 0	KEG6 0	KEG5 0	KEG4 0	KEG3 0	KEG2 0	KEG1 0	KEG0 0
0×0B	KEY_EVENT_H	Key event register H	KEH7 0	KEH6 0	KEH5 0	KEH4 0	KEH3 0	KEH2 0	KEH1 0	KEH0 0
0×0C	KEY_EVENT_I	Key event register I	KEI7 0	KEI6 0	KEI5 0	KEI4 0	KEI3 0	KEI2 0	KEI1 0	KEI0 0
0×0D	KEY_EVENT_J	Key event register J	KEJ7 0	KEJ6 0	KEJ5 0	KEJ64 0	KEJ3 0	KEJ2 0	KEJ1 0	KEJ0 0
0×0E	KP_LCK_TIMER	Keypad lock 1 to lock 2 timer	KL7	KL6	KL5	KL4	KL3	KL2	KL1	KL0
0×0F	Unlock1	Unlock key 1	UK1_7	UK1_6	UK1_5	UK1_4	UK1_3	UK1_2	UK1_1	UK1_0
0×10	Unlock2	Unlock key2	UK2_7	UK2_6	UK2_5	UK2_4	UK2_3	UK2_2	UK2_1	UK2_0
0×11	GPIO_INT_STAT1	GPIO interrupt status	R7IS 0	R6IS 0	R5IS 0	R4IS 0	R3IS 0	R2IS 0	R1IS 0	R0IS 0
0×12	GPIO_INT_STAT2	GPIO interrupt status	C7IS 0	C6IS 0	C5IS 0	C4IS 0	C3IS 0	C2IS 0	C1IS 0	C0IS 0

Table 3. Register Descriptions (continued)

ADDRESS	REGISTER NAME	REGISTER DESCRIPTION	7	6	5	4	3	2	1	0
0×13	GPIO_INT_STAT3	GPIO interrupt status	N/A 0	N/A 0	N/A 0	N/A 0	N/A 0	N/A 0	C9IS 0	C8IS 0
0×14	GPIO_DAT_STAT1 (read twice to clear)	GPIO data status	R7DS	R6DS	R5DS	R4DS	R3DS	R2DS	R1DS	R0DS
0×15	GPIO_DAT_STAT2 (read twice to clear)	GPIO data status	C7DS	C6DS	C5DS	C4DS	C3DS	C2DS	C1DS	C0DS
0×16	GPIO_DAT_STAT3 (read twice to clear)	GPIO data status	N/A 0	N/A 0	N/A 0	N/A 0	N/A 0	N/A 0	C9DS	C8DS
0×17	GPIO_DAT_OUT1	GPIO data out	R7DO 0	R6DO 0	R5DO 0	R4DO 0	R3DO 0	R2DO 0	R1DO 0	R0DO 0
0×18	GPIO_DAT_OUT2	GPIO data out	C7DO 0	C6DO 0	C5DO 0	C4DO 0	C3DO 0	C2DO 0	C1DO 0	C0DO 0
0×19	GPIO_DAT_OUT3	GPIO data out	N/A 0	N/A 0	N/A 0	N/A 0	N/A 0	N/A 0	C9DO 0	C8DO 0
0×1A	GPIO_INT_EN1	GPIO interrupt enable	R7IE 0	R6IE 0	R5IE 0	R4IE 0	R3IE 0	R2IE 0	R1IE 0	R0IE 0
0×1B	GPIO_INT_EN2	GPIO interrupt enable	C7IE 0	C6IE 0	C5IE 0	C4IE 0	C3IE 0	C2IE 0	C1IE 0	C0IE 0
0×1C	GPIO_INT_EN3	GPIO interrupt enable	N/A 0	N/A 0	N/A 0	N/A 0	N/A 0	N/A 0	C9IE 0	C8IE 0
0×1D	KP_GPIO1	Keypad or GPIO selection 0: GPIO 1: KP matrix	ROW7 0	ROW6 0	ROW5 0	ROW4 0	ROW3 0	ROW2 0	ROW1 0	ROW0 0
0×1E	KP_GPIO2	Keypad or GPIO selection 0: GPIO 1: KP matrix	COL7 0	COL6 0	COL5 0	COL4 0	COL3 0	COL2 0	COL1 0	COL0 0
0×1F	KP_GPIO3	Keypad or GPIO selection 0: GPIO 1: KP matrix	N/A 0	N/A 0	N/A 0	N/A 0	N/A 0	N/A 0	COL9 0	COL8 0
0×20	GPI_EM1	GPI event mode 1	ROW7 0	ROW6 0	ROW5 0	ROW4 0	ROW3 0	ROW2 0	ROW1 0	ROW0 0
0×21	GPI_EM2	GPI event mode 2	COL7 0	COL6 0	COL5 0	COL4 0	COL3 0	COL2 0	COL1 0	COL0 0
0×22	GPI_EM3	GPI event mode 3	N/A 0	N/A 0	N/A 0	N/A 0	N/A 0	N/A 0	COL9 0	COL8 0
0×23	GPIO_DIR1	GPIO data direction 0: input 1: output	R7DD 0	R6DD 0	R5DD 0	R4DD 0	R3DD 0	R2DD 0	R1DD 0	R0DD 0
0×24	GPIO_DIR2	GPIO data direction 0: input 1: output	C7DD 0	C6DD 0	C5DD 0	C4DD 0	C3DD 0	C2DD 0	C1DD 0	C0DD 0
0×25	GPIO_DIR3	GPIO data direction 0: input 1: output	N/A 0	N/A 0	N/A 0	N/A 0	N/A 0	N/A 0	C9DD 0	C8DD 0
0×26	GPIO_INT_LVL 1	GPIO edge/level detect 0: low 1: high	R7IL 0	R6IL 0	R5IL 0	R4IL 0	R3IL 0	R2IL 0	R1IL 0	R0IL 0
0×27	GPIO_INT_LVL 2	GPIO edge/level detect 0: low 1: high	C7IL 0	C6IL 0	C5IL 0	C4IL 0	C3IL 0	C2IL 0	C1IL 0	C0IL 0

Table 3. Register Descriptions (continued)

ADDRESS	REGISTER NAME	REGISTER DESCRIPTION	7	6	5	4	3	2	1	0
0×28	GPIO_INT_LVL 3	GPIO edge/level detect 0: low 1: high	N/A 0	N/A 0	N/A 0	N/A 0	N/A 0	N/A 0	C9IL 0	C8IL 0
0×29	DEBOUNCE_DIS 1	Debounce disable 0: enabled 1: disabled	R7DD 0	R6DD 0	R5DD 0	R4DD 0	R3DD 0	R2DD 0	R1DD 0	R0DD 0
0×2A	DEBOUNCE_DIS 2	Debounce disable 0: enabled 1: disabled	C7DD 0	C6DD 0	C5DD 0	C4DD 0	C3DD 0	C2DD 0	C1DD 0	C0DD 0
0×2B	DEBOUNCE_DIS 3	Debounce disable 0: enabled 1: disabled	Debounce time bits			N/A 0	N/A 0	N/A 0	C9DD 0	C8DD 0
0×2C	GPIO_PULL1	GPIO pullup 0: pullup enabled 1: pullup disabled	R7PD 0	R6PD 0	R5PD 0	R4PD 0	R3PD 0	R2PD 0	R1PD 0	R0PD 0
0×2D	GPIO_PULL2	GPIO pullup 0: pullup enabled 1: pullup disabled	C7PD 0	C6PD 0	C5PD 0	C4PD 0	C3PD 0	C2PD 0	C1PD 0	C0PD 0
0×2E	GPIO_PULL3	GPIO pullup 0: pullup enabled 1: pullup disabled	N/A 0	N/A 0	N/A 0	N/A 0	N/A 0	N/A 0	C9PD 0	C8PD 0
0×2F	Reserved									

Configuration Register (Address 0×01)

BIT	NAME	DESCRIPTION
7	AI	Auto-increment for read and write operations 0 = disabled 1 = enabled
6	GPI_E_CFG	GPI event mode configuration 0 = GPI events are tracked when keypad is locked 1 = GPI events are not tracked when keypad is locked
5	OVR_FLOW_M	Overflow mode 0 = disabled; overflow data is lost 1 = enabled.
4	INT_CFG	Overflow data shifts with last event pushing first event out interrupt configuration. 0 = processor interrupt remains asserted (or low) if host tries to clear interrupt while there is still a pending key press, key release or GPI interrupt 1 = processor interrupt is deasserted for 50 µs and reassert with pending interrupts
3	OVR_FLOW_IEN	Overflow interrupt enable 0 = disabled 1 = enabled
2	K_LCK_IEN	Keypad lock interrupt enable 0 = disabled 1 = enabled
1	GPI_IEN	GPI interrupt enable to host processor 0 = disabled 1 = enabled Can be used to mask interrupts

BIT	NAME	DESCRIPTION
0	KE_IEN	Key events interrupt enable to host processor 0 = disabled 1 = enabled Can be used to mask interrupts

Bit 7 in this register is used to determine the programming mode. If it is low, all data bytes are written to the registers defined command byte. If bit 7 is high, the value of the command byte is automatically incremented after the byte is written, and the next data byte is stored in the corresponding register. Registers are written in the sequence shown in Table 3. Once the GPIO_PULL3 register (0×2E) is written to, the command byte returns to 0 (Configuration register). Registers 0 and 2F are reserved and a command byte that references these registers is not acknowledged by the TCA8418E.

The keypad lock interrupt enable determines if the interrupt pin is asserted when the key lock interrupt (see Interrupt Status Register) bit is set.

Interrupt Status Register, INT_STAT (Address 0×02)

BIT	NAME	DESCRIPTION
7	N/A	Always 0
6	N/A	Always 0
5	N/A	Always 0
4	CAD_INT	CTRL-ALT-DEL key sequence status. Requires writing a 1 to clear interrupts. 0 = interrupt not detected 1 = interrupt detected
3	OVR_FLOW_INT	Overflow interrupt status. Requires writing a 1 to clear interrupts. 0 = interrupt not detected 1 = interrupt detected
2	K_LCK_INT	Keypad lock interrupt status. This is the interrupt to the processor when the keypad lock sequence is started. Requires writing a 1 to clear interrupts. 0 = interrupt not detected 1 = interrupt detected
1	GPI_INT	GPI interrupt status. Requires writing a 1 to clear interrupts. 0 = interrupt not detected 1 = interrupt detected Can be used to mask interrupts
0	K_INT	Key events interrupt status. Requires writing a 1 to clear interrupts. 0 = interrupt not detected 1 = interrupt detected

Key Lock and Event Counter Register, KEY_LCK_EC (Address 0×03)

BIT	NAME	DESCRIPTION
7	N/A	Always 0
6	K_LCK_EN	Key lock enable 0 = disabled 1 = enabled
5	LCK2	Keypad lock status 0 = unlock (if LCK1 is 0 too) 1 = locked (if LCK1 is 1 too)
4	LCK1	Keypad lock status 0 = unlock (if LCK2 is 0 too) 1 = locked (if LCK2 is 1 too)
3	KEC3	Key event count, Bit 3
2	KEC2	Key event count, Bit 2

BIT	NAME	DESCRIPTION
1	KEC1	Key event count, Bit 1
0	KEC0	Key event count, Bit 0

KEC[3:0]: indicates how many registers have values in it. For example, KS(0000) = 0 events, KS(0001) = 1 event and KS(1010) = 10 events. As interrupts happen (press or release), the count increases accordingly.

Key Event Registers (FIFO), KEY_EVENT_A–J (Address 0×04–0×0D)

ADDRESS	REGISTER NAME(1)	REGISTER DESCRIPTION	BIT							
			7	6	5	4	3	2	1	0
0×04	KEY_EVENT_A	Key event register A	KEA 7 0	KEA6 0	KEA 5 0	KEA4 0	KEA3 0	KEA 2 0	KEA1 0	KEA 0 0

(1) Only KEY_EVENT_A register is shown

These registers – KEY_EVENT_A-J – function as a FIFO stack which can store up to 10 key presses and releases. The user first checks the INT_STAT register to see if there are any interrupts. If so, then the Key Lock and Event Counter Register (KEY_LCK_EC, register 0x03) is read to see how many interrupts are stored. The INT_STAT register is then read again to ensure no new events have come in. The KEY_EVENT_A register is then read as many times as there are interrupts. Each time a read happens, the count in the KEY_LCK_EC register reduces by 1. The data in the FIFO also moves down the stack by 1 too (from KEY_EVENT_J to KEY_EVENT_A). Once all events have been read, the key event count is at 0 and then KE_INT bit can be cleared by writing a ‘1’ to it.

In the KEY_EVENT_A register, KEA[6:0] indicates the key # pressed or released. A value of 0 to 80 indicate which key has been pressed or released in a keypad matrix. Values of 97 to 114 are for GPI events.

Bit 7 or KEA[7] indicate if a key press or key release has happened. A ‘0’ means a key release happened. A ‘1’ means a key has been pressed (which can be cleared on a read).

For example, 3 key presses and 3 key releases are stored as 6 words in the FIFO. As each word is read, the user knows if it is a key press or key release that occurred. Key presses such as CTRL+ALT+DEL are stored as 3 simultaneous key presses. Key presses and releases generate key event interrupts. The KE_INT bit and /INT pin will not cleared until the FIFO is cleared of all events.

All registers can be read but for the purpose of the FIFO, the user should only read KEY_EVENT_A register. Once all the events in the FIFO have been read, reading of KEY_EVENT_A register will yield a zero value.

Keypad Lock1 to Lock2 Timer Register, KP_LCK_TIMER (Address 0×0E)

ADDRESS	REGISTER NAME(1)	REGISTER DESCRIPTION	BIT							
			7	6	5	4	3	2	1	0
0×0E	KP_LCK_TIMER	Keypad lock 1 to lock 2 timer	KL7	KL6	KL5	KL4	KL3	KL2	KL1	KL0

(1) Only KEY_EVENT_A register is shown

KL[2:0] are for the Lock1 to Lock2 timer

KL[7:3] are for the interrupt mask timer

The interrupt mask timer should be set for the time it takes for the LCD to dim or turn off.

Unlock1 and Unlock2 Registers, UNLOCK1/2 (Address o0×0F)

ADDRESS	REGISTER NAME(1)	REGISTER DESCRIPTION	BIT							
			7	6	5	4	3	2	1	0
0×0F	Unlock1	Unlock key 1	UK1_ 7	UK1_ 6	UK1 _5	UK1_ 4	UK1_ 3	UK1 _2	UK1_ 1	UK1 _0
0×10	Unlock2	Unlock key 2	UK2_ 7	UK2_ 6	UK2 _5	UK2_ 4	UK2_ 3	UK2 _2	UK2_ 1	UK2 _0

(1) Only KEY_EVENT_A register is shown

UK1[6:0] contains the key number used to unlock key 1

UK2[6:0] contains the key number used to unlock key 2

A ‘0’ in either register means it is disabled. It lasts up to 7 seconds. Needs a second timer up to 31 seconds? The keypad lock interrupt mask timer generates a first interrupt (K_INT) and then waits for a programmed time before generating a second interrupt. A second interrupt can only be generated when a timer is enabled due to an unlock sequence being pressed. The second interrupt is a key lock interrupt. When the interrupt mask timer is disabled (‘0’), a key lock interrupt will trigger only when the correct and complete unlock sequence is completed.

GPIO Interrupt Status Registers, GPIO_INT_STAT1–3 (Address 0×11–0×13)

These registers are used to check GPIO interrupt status and are cleared on read.

GPIO Data Status Registers, GPIO_DAT_STAT1–3 (Address 0×14–0×16)

These registers show GPIO state when read for inputs and outputs.

GPIO Data Out Registers, GPIO_DAT_OUT1–3 (Address 0×17–0×19)

These registers contain GPIO data to be written to GPIO out driver; inputs are not affected. This is needed so that the value can be written prior to being set as an output.

GPIO Interrupt Enable Registers, GPIO_INT_EN1–3 (Address 0×1A–0×1C)

These registers enable interrupts for GP inputs only.

Keypad or GPIO Selection Registers, KP_GPIO1–3 (Address 0×1D–0×1F)

A bit value of '0' in any of the unreserved bits puts the corresponding pin in GPIO mode. A '1' in any of these bits puts the pin in keyscan mode and configured as a row or column accordingly.

GPI Event Mode Registers, GPI_EM1–3 (Address 0×20–0×22)

A bit value of '0' in any of the unreserved bits indicates that it is not part of the event FIFO. A '1' in any of these bits means it is part of the event FIFO. GPIO Data Direction Registers (GPIO_DIR1-3, Register address of 0x23-0x25) A bit value of '0' in any of the unreserved bits sets the corresponding pin as an input. A '1' in any of these bits sets the pin as an output. GPIO Edge/Level Detect Registers (GPIO_INT_LVL1-3, Register address of 0x26-0x28) A bit value of '0' indicates that interrupt will be triggered on a high-to-low transition for the inputs in GPIO mode. A bit value of '1' indicates that interrupt will be triggered on a low-to-high value for the inputs in GPIO mode.

GPIO Data Direction Registers, GPIO_DIR1–3 (Address 0×23–0×25)

A bit value of '0' in any of the unreserved bits sets the corresponding pin as an input. A '1' in any of these bits sets the pin as an output. GPIO Edge/Level Detect Registers (GPIO_INT_LVL1-3, Register address of 0x26-0x28) A bit value of '0' indicates that interrupt will be triggered on a high-to-low transition for the inputs in GPIO mode. A bit value of '1' indicates that interrupt will be triggered on a low-to-high value for the inputs in GPIO mode.

GPIO Edge/Level Detect Registers, GPIO_INT_LVL1–3 (Address 0×26–0×28)

A bit value of '0' indicates that interrupt will be triggered on a high-to-low transition for the inputs in GPIO mode. A bit value of '1' indicates that interrupt will be triggered on a low-to-high value for the inputs in GPIO mode.

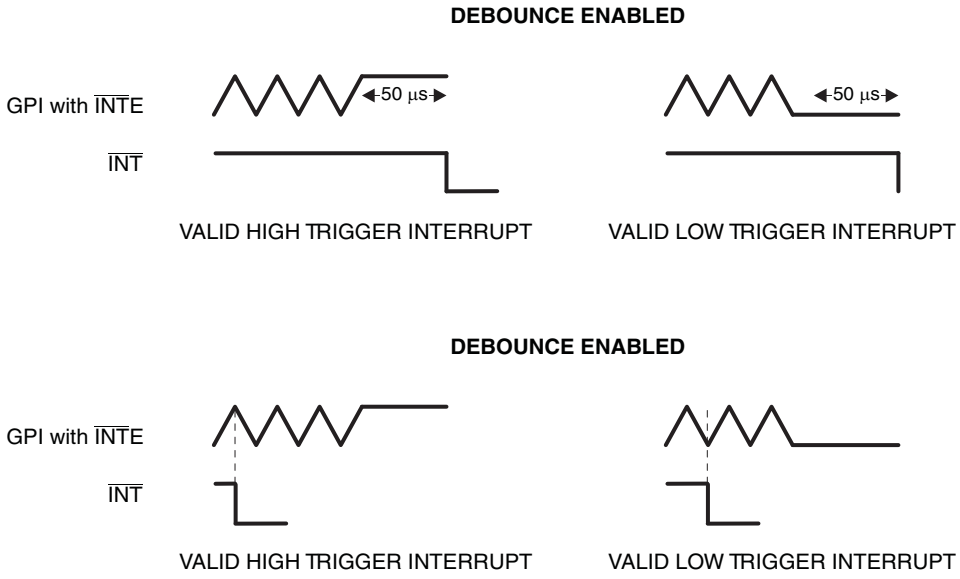
Debounce Disable Registers, DEBOUNCE_DIS1–3 (Address 0×29–0×2B)

This is for pins configured as inputs. A bit value of ‘0’ in any of the unreserved bits disables the debounce while a bit value of ‘1’ enables the debounce.

In register DEBOUNCE_DIS3 [7:5] can be used to program the value of the debounce time.

ADDRESS	REGISTER NAME(1)	REGISTER DESCRIPTION	BIT							
			7	6	5	4	3	2	1	0
0×2B	DEBOUNCE_DIS 3	Debounce disable 0: enabled 1: disabled	debounce time bits			N/A 0	N/A 0	N/A 0	C9DD 0	C8DD 0

(1) Only KEY_EVENT_A register is shown



Debounce disable will have the same effect for GPI mode or for rows in keypad scanning mode. The reset line always has a 50-µs debounce time.

The debounce time for inputs is the time required for the input to be stable to be noticed. This time is 50 µs.

The debounce time for the keypad is for the columns only. The minimum time is 20 ms. All columns are scanned once every 20 ms to detect any key presses. Two full scans are required to see if any keys were pressed. If the first scan is done just after a key press, it will take 20 ms to detect the key press. If the first scan is down much later than the key press, it will take 40 ms to detect a key press.

GPIO Pull Disable Register, GPIO_PULL1–3 (Address 0×2C–0×2E)

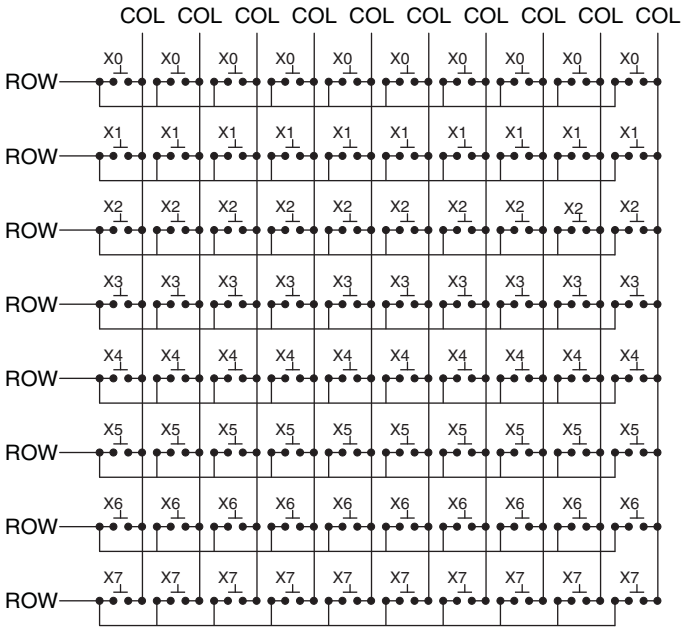
This register enables or disables pullup registers from inputs.

Typical Application

Figure 8 shows an application in which the TCA8418E can be used.

placeholder

Figure 8. Typical Application



The 18 GPIOs can be configured to support up to 80 keys. The GPIOs are programmed into rows (maximum of 8) and columns (maximum of 10) to support a keypad. This is done through writing to “Keypad or GPIO Selection” registers (0x1D – 0x1F). The keypad in idle mode will be configured as Columns being driven low and Rows as inputs with pull-ups.

When there is a key press or multiple key presses (Short between Column and Row), it will trigger an internal state machine interrupt. The row that has a pressed key can be determined through reading the “GPIO Data Status” registers (0x14-0x16).After that, the state machine starts a keyscan cycle to determine the column of the key that was pressed. The state machine sets one column as an output low and all other columns as high. The state machine will then walk a zero across the applicable row to determine what keys are being pressed.

Once a key has been pressed for 10ms, the state machine will set the appropriate key/s in the Key Event Status register with the key-pressed bit set (bit 7). If the K_IEN is set it will then set KE_INT and generate an interrupt to the host processor. The state machine will continue to poll while there are keys pressed. If a key/s that was in the key pressed register is released for 10ms or greater, the state machine will set the appropriate keys in the Key Event Status register with the key pressed bit cleared. If K_IEN is set it will set the K_INT and generate an interrupt to the host processor.

After receiving an interrupt, the host processor will first read the Interrupt Status register to determine what interrupt caused the processor interrupt. It will then read the Key Event Register to see what keys where pressed/released (Bits will then automatically clear on read in those registers). The processor will then write a 1 to the interrupt bit in the interrupt register to clear it and release the host interrupt to the processor. The processor can see the status of what keys are pressed at any point by reading the KEY_EVENT_A register (FIFO).

See Key Event Registers (FIFO) for more information.

When all Key_Event Registers are full, any additional events with set the OVR_FLOW_INT bit to 1. This will also trigger an interrupt to the processor. When the FIFO is not full, new events are added to the next empty Key_Event register in line. The OVR_FLOW_M bit sets the mode of operation during overflows. Clearing this bit will cause new incoming events to be ignored and discarded. Setting this bit will overwrite old data with new data starting with the first event.

Keypad Lock/Unlock

This user can lock the keypad through the lock/unlock feature in this device. Once the keypad is locked, it can prevent the generation of key event interrupts and recorded key events. The unlock keys can be programmed with any value of the keys in the keypad matrix or any GPI values that are part of the key event table. When the keypad lock interrupt mask timer is enabled, the user will need to press two specific keys before an keylock interrupt is generated or keypad events are recorded. After the keypad is locked, a key event interrupt is generated any time a user presses a key. This first interrupt also triggers the processor to turn on the LCD and display the unlock message. The processor will then read the lock status register to see if the keypad is unlocked. The next interrupt (keylock interrupt) will not be generated unless both unlock keys sequences are correct. If correct Unlock keys are not pressed before the mask timer expires, the state machine will start over again.

Ghosting

Supports multiple key presses accurately. Applications requiring three-key combinations (such as <Ctrl><Alt><Del>) must ensure that the three keys are wired in appropriate key positions to avoid ghosting (or appearing like a 4th key has been pressed)

GPI Events

A column or row configured as GPI can be programmed to be part of the Key Event Table, hence becomes also capable of generating Key Event Interrupt. A key Event Interrupt caused by a GPI follow the same process flow as a Key Event Interrupt caused by a Key press.

GPIs configured as part of the Key Event Table allows for single key switches to be monitored as well as other GPI interrupts. As part of the Event Table, GPIs are represented with decimal value of 97 (0x61 or 1100001) and run through decimal value of 114 (0x72 or 1110010).

For a GPI that is set as active high, and is enabled in the Key Event Table, the state-machine will add an event to the event count and event table whenever that GPI goes high. If the GPI is set to active low, a transition from high to low will be considered a press and will also be added to the event count and event table. Once the interrupt state has been met, the state machine will internally set an interrupt for the opposite state programmed in the register to avoid polling for the released state, hence saving current. Once the released state is achieved, it will add it to the event table. The press and release will still be indicated by bit 7 in the event register.

The GPI Events can also be used as unlocked sequences. When the GPI_EM bit is set, GPI events will not be tracked when the keypad is locked. GPI_EM bit must be cleared for the GPI events to be tracked in the event counter and table when the keypad is locked.

Bus Transactions

Data is exchanged between the master and TCA8418E through write and read commands.

Writes

Data is transmitted to the TCA8418E by sending the device address and setting the least significant bit (LSB) to a logic 0. The command byte is sent after the address and determines which register receives the data that follows the command byte. There is no limitation on the number of data bytes sent in one write transmission.

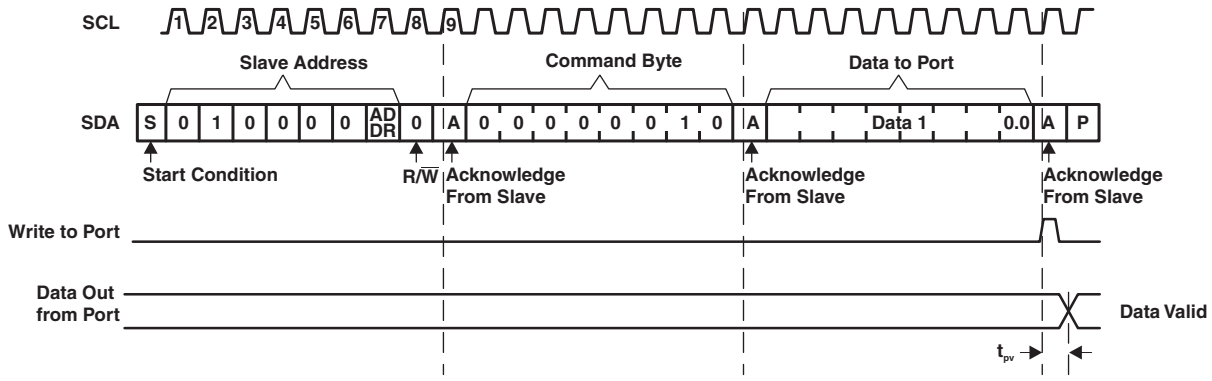


Figure 9. Write to Output Port Register

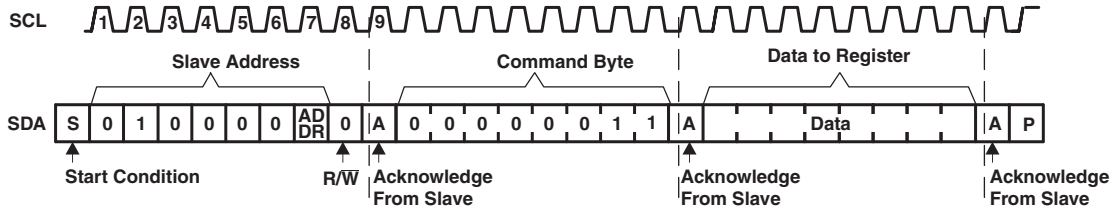


Figure 10. Write to Configuration or Polarity Inversion Register

Reads

The bus master first must send the TCA8418E address with the LSB set to a logic 0. The command byte is sent after the address and determines which register is accessed. After a restart, the device address is sent again but, this time, the LSB is set to a logic 1. Data from the register defined by the command byte then is sent by the TCA8418E (see Figure 11 and Figure 12). Data is clocked into the register on the rising edge of the ACK clock pulse.

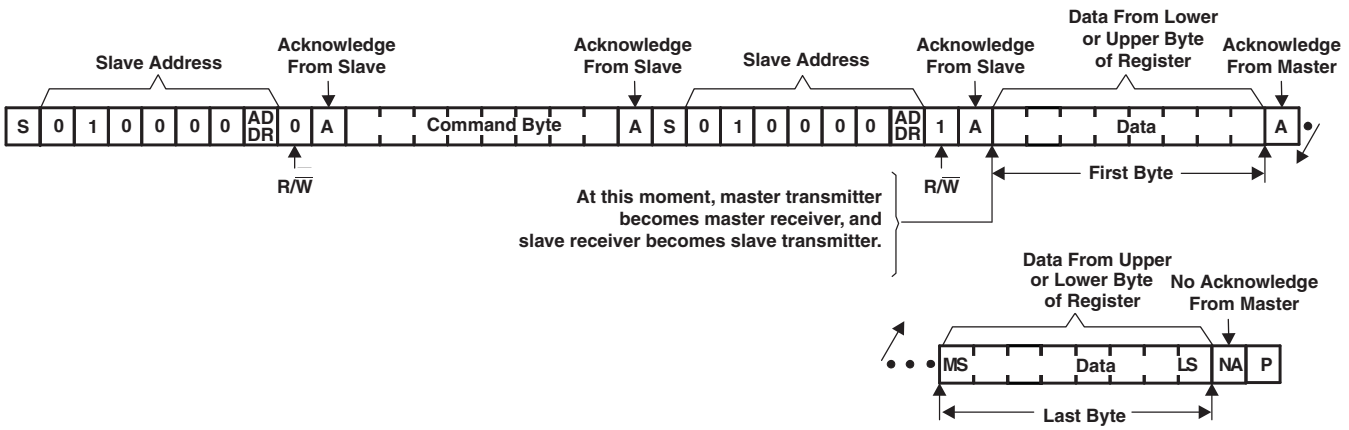


Figure 11. Read From Register

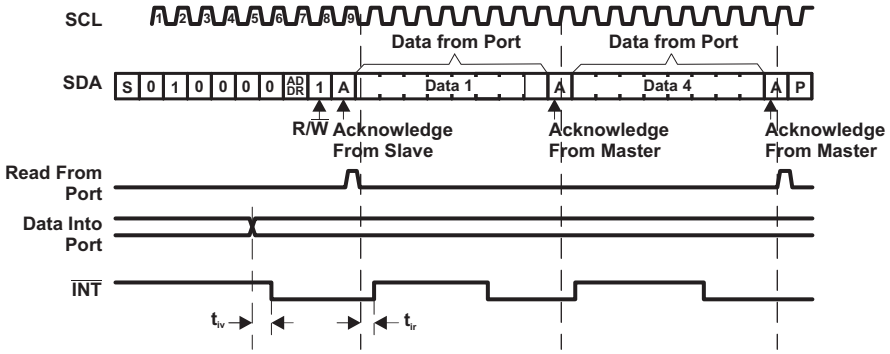
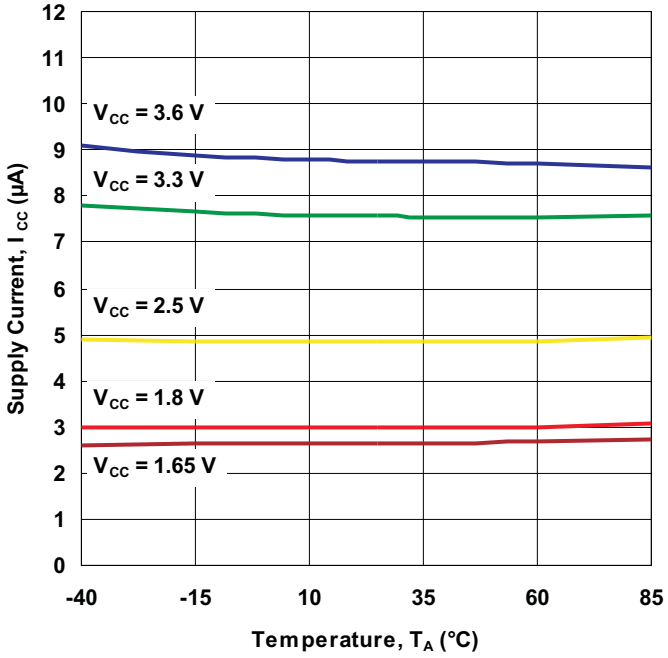


Figure 12. Read From Input Port Register

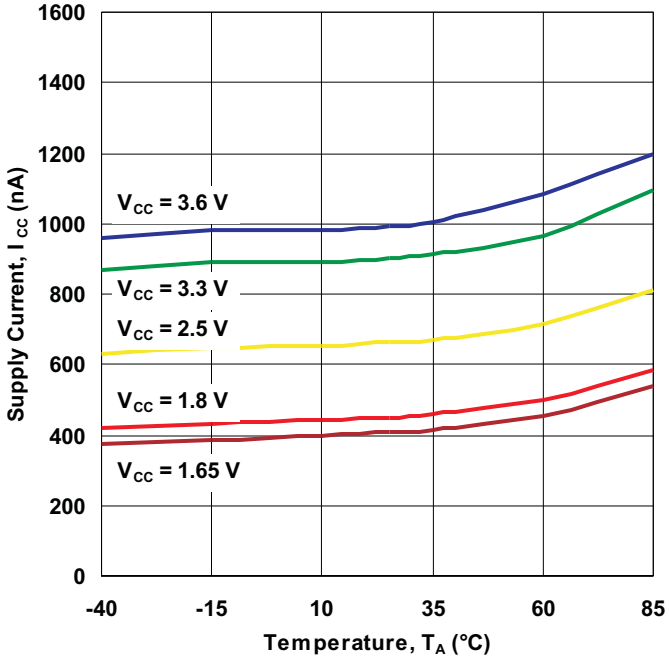
TYPICAL CHARACTERISTICS

T_A = 25°C (unless otherwise noted)

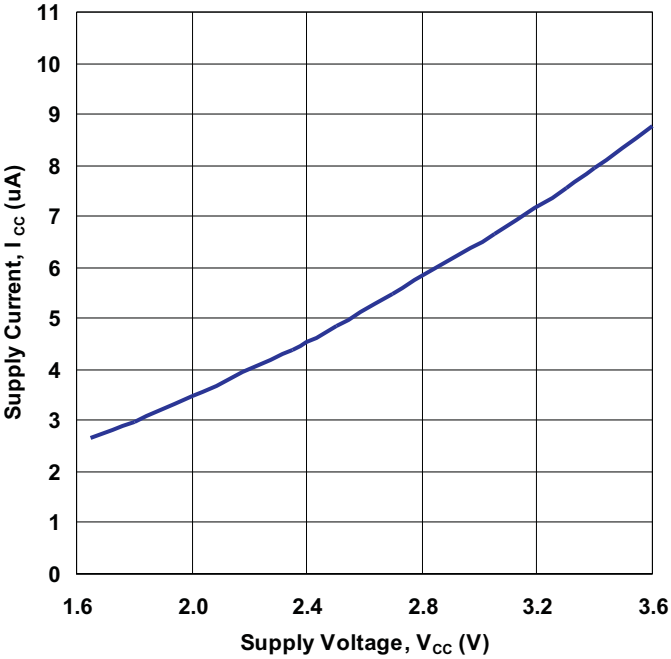
SUPPLY CURRENT
vs
TEMPERATURE



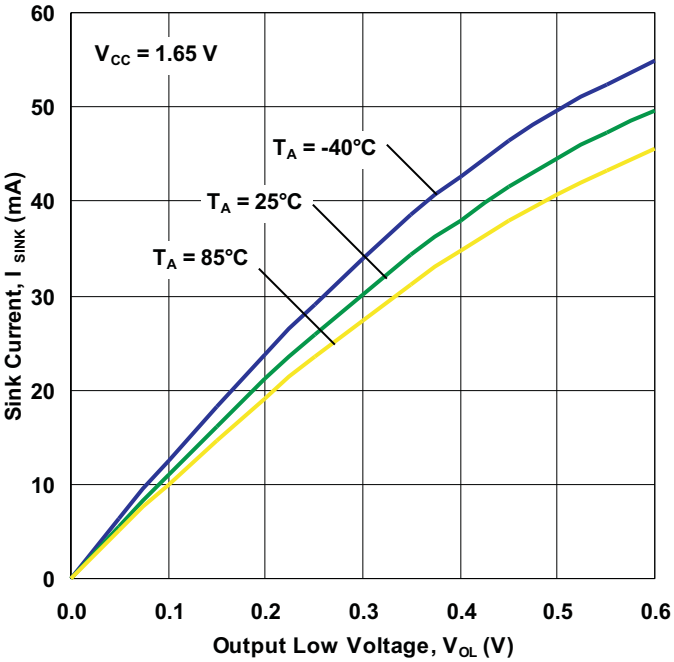
STANDBY SUPPLY CURRENT
vs
TEMPERATURE



SUPPLY CURRENT
vs
SUPPLY VOLTAGE

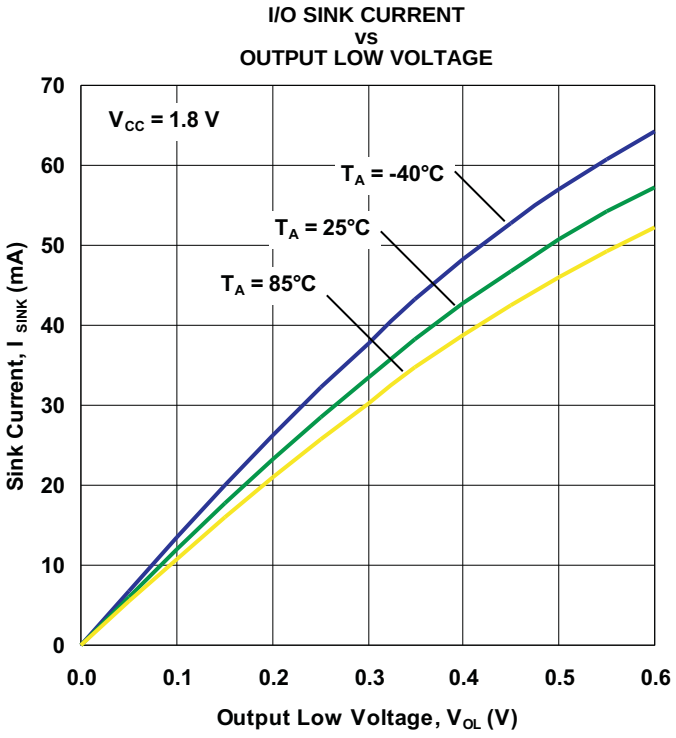


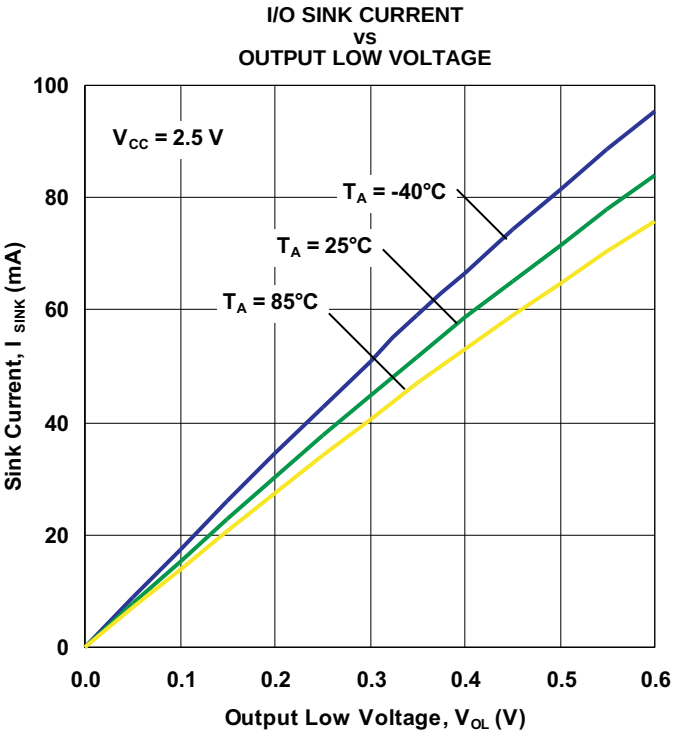
I/O SINK CURRENT
vs
OUTPUT LOW VOLTAGE

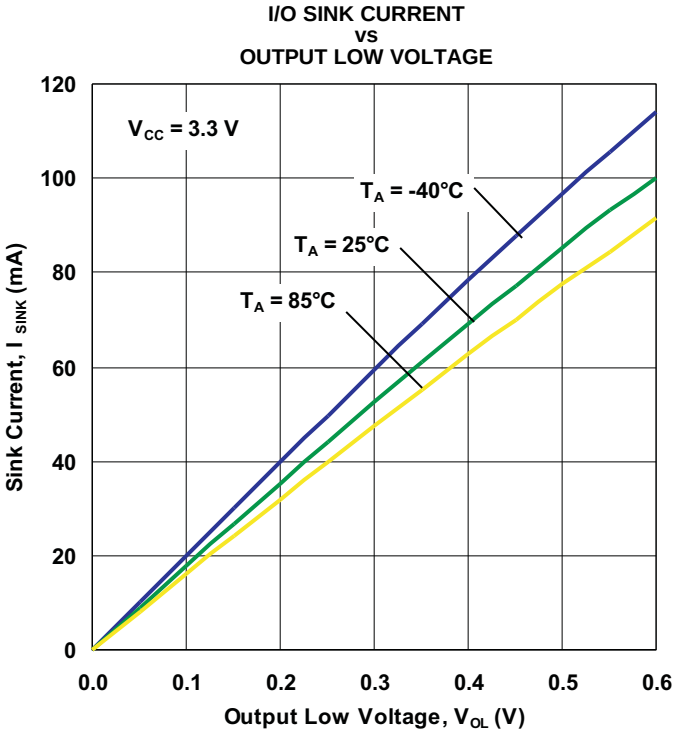


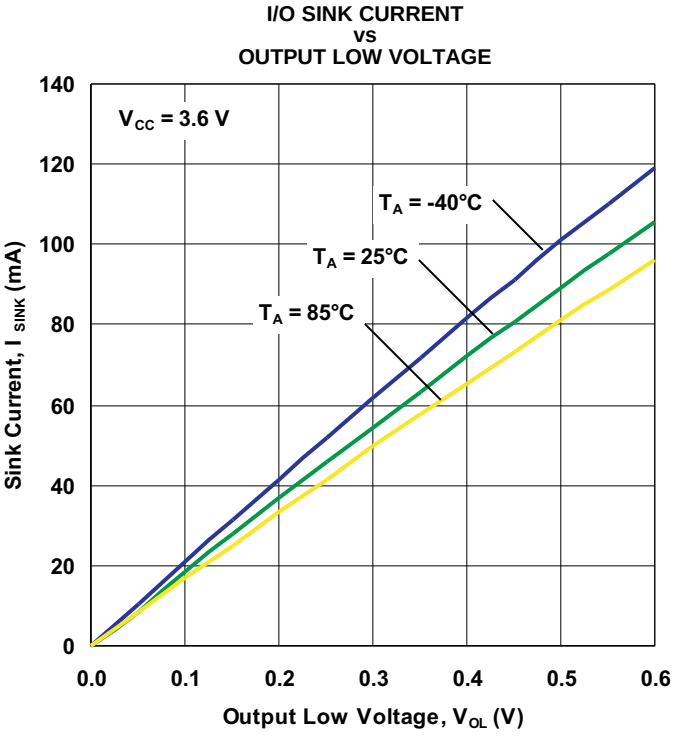
TYPICAL CHARACTERISTICS (continued)

T_A = 25°C (unless otherwise noted)





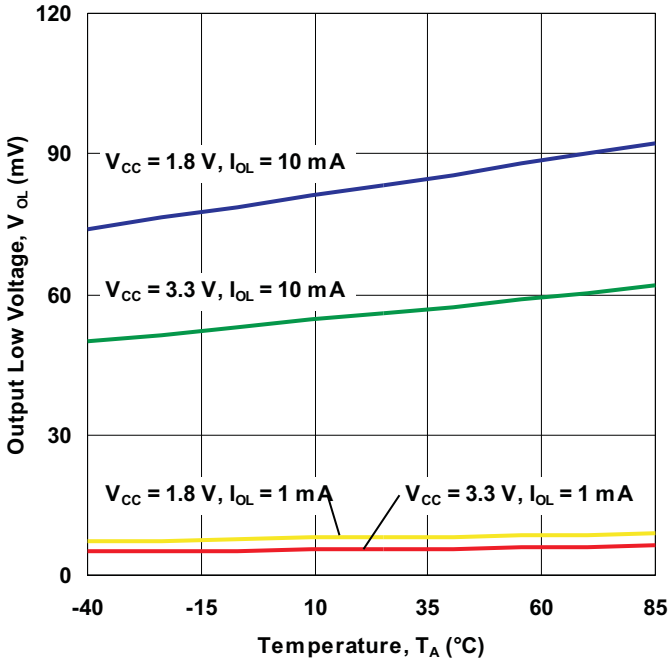




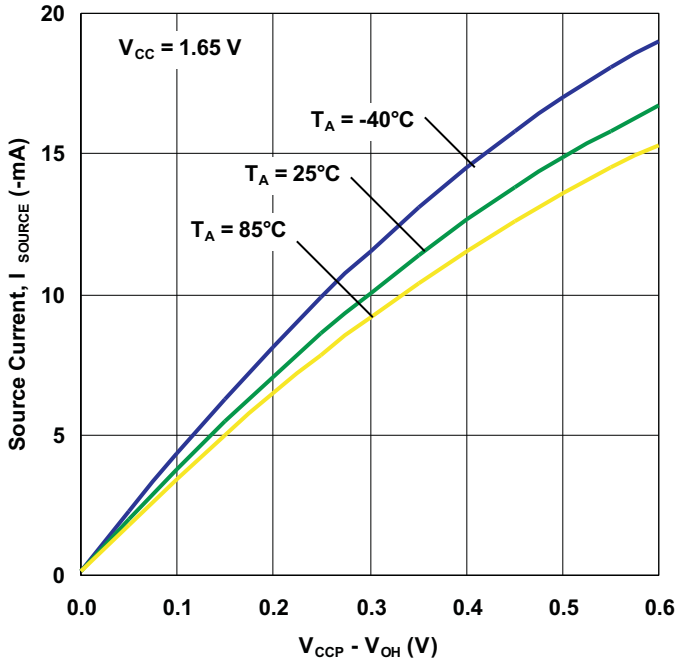
TYPICAL CHARACTERISTICS (continued)

T_A = 25°C (unless otherwise noted)

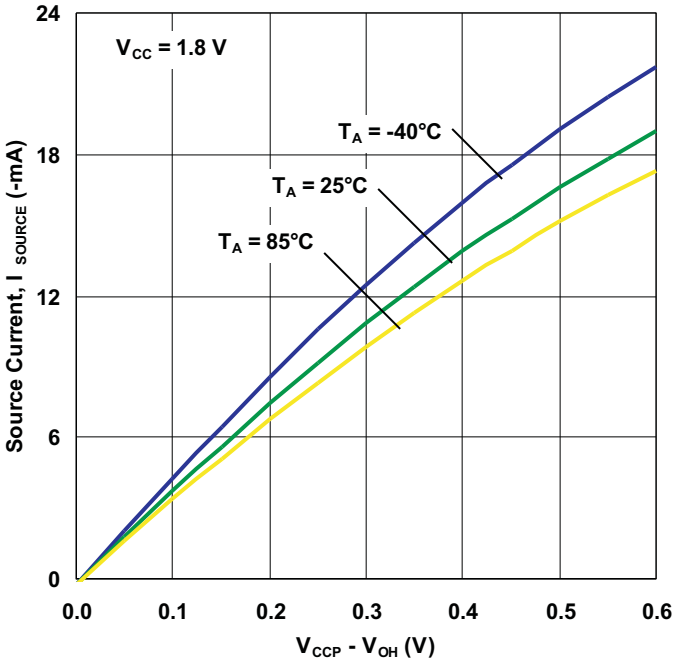
I/O LOW VOLTAGE vs TEMPERATURE



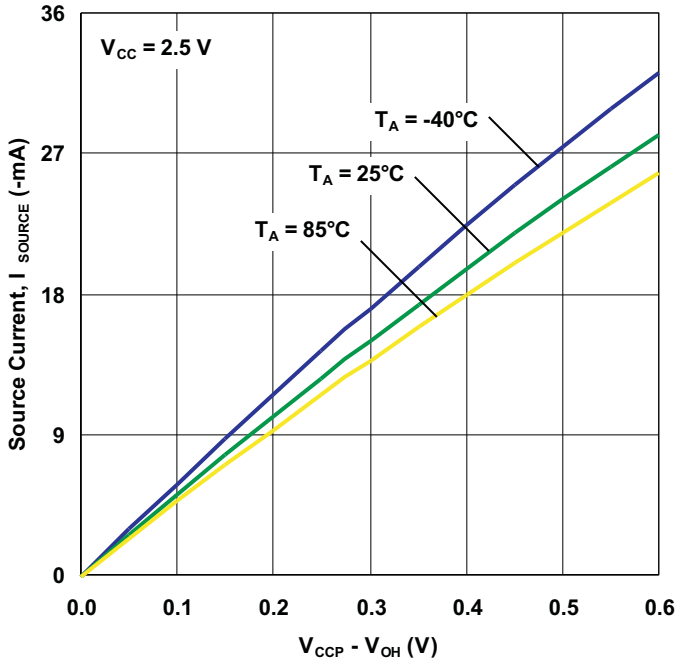
I/O SOURCE CURRENT vs OUTPUT HIGH VOLTAGE



I/O SOURCE CURRENT vs OUTPUT HIGH VOLTAGE

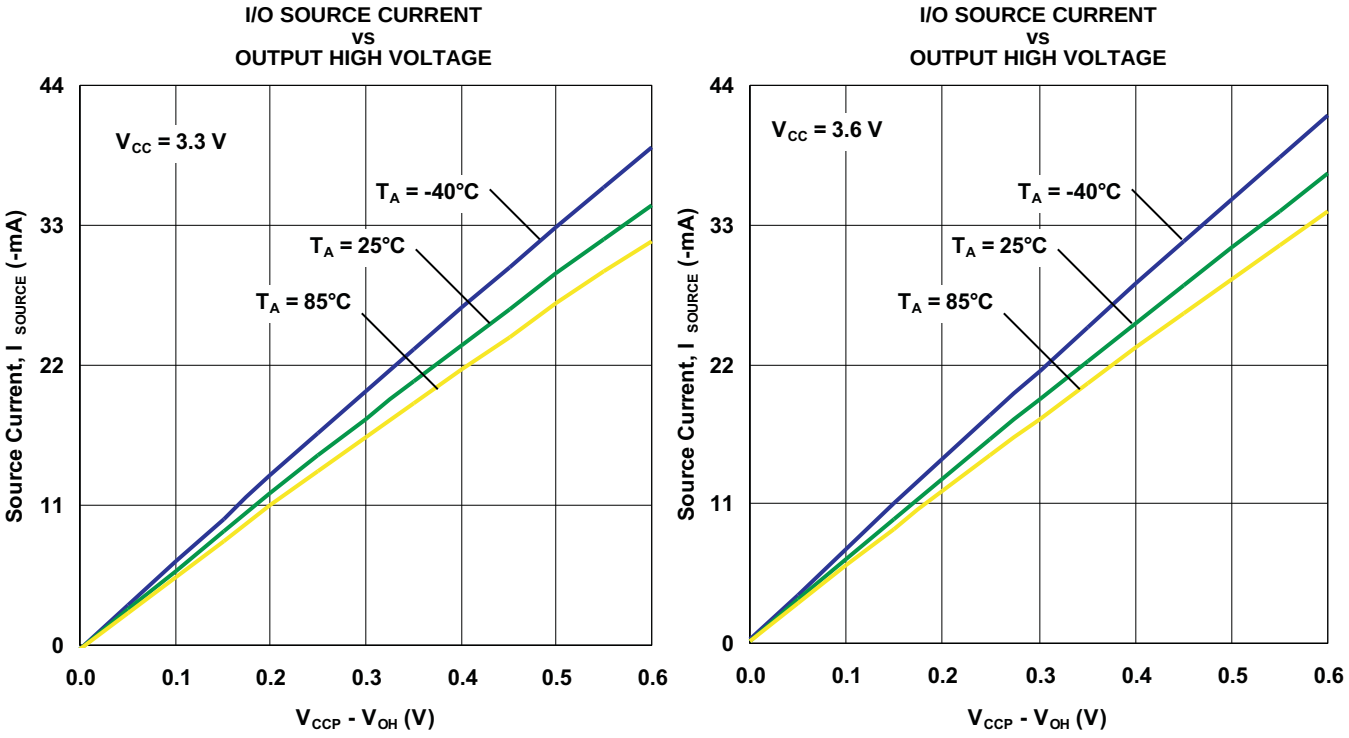


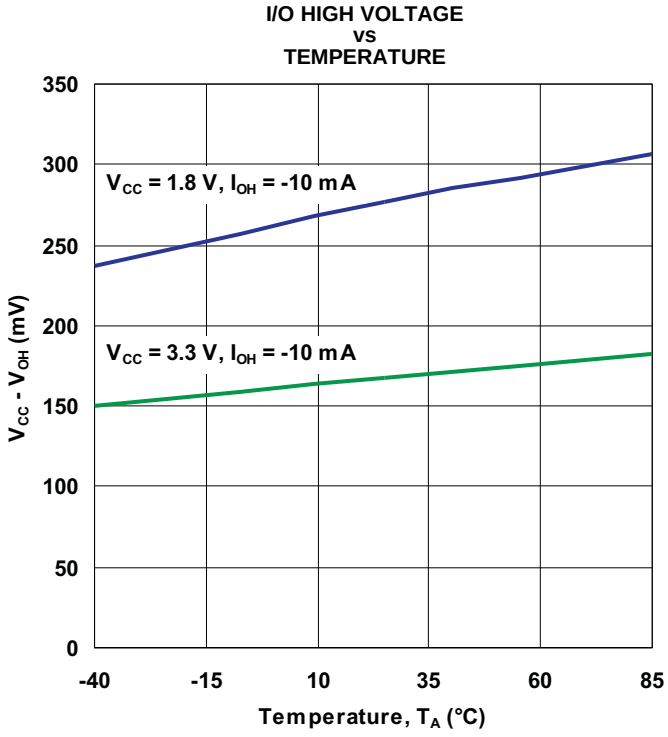
I/O SOURCE CURRENT vs OUTPUT HIGH VOLTAGE



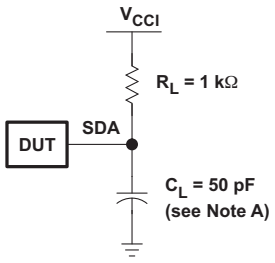
TYPICAL CHARACTERISTICS (continued)

T_A = 25°C (unless otherwise noted)

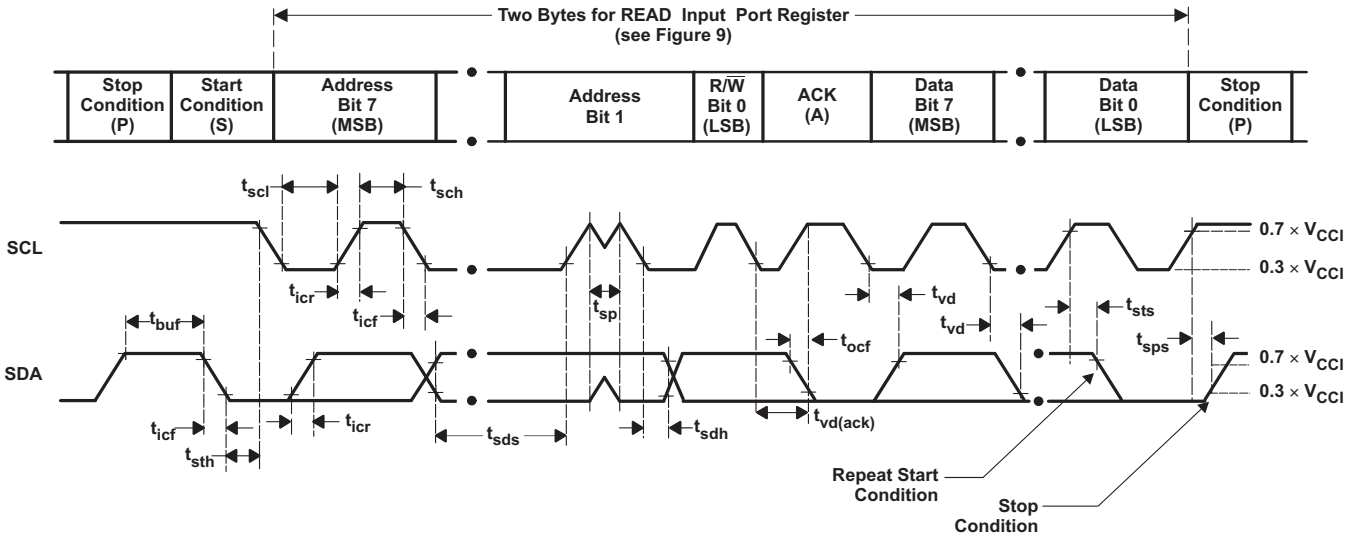




PARAMETER MEASUREMENT INFORMATION



SDA LOAD CONFIGURATION



VOLTAGE WAVEFORMS

BYTE	DESCRIPTION
1	I^2C address
2	Input register port data

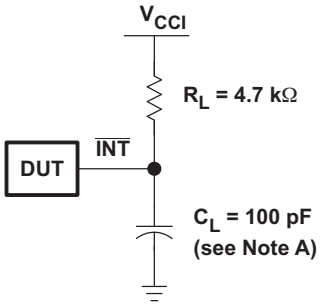
A. C_L includes probe and jig capacitance. t_{ocf} is measured with C_L of 10 pF or 400 pF.

B. All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f ≤ 30 ns.

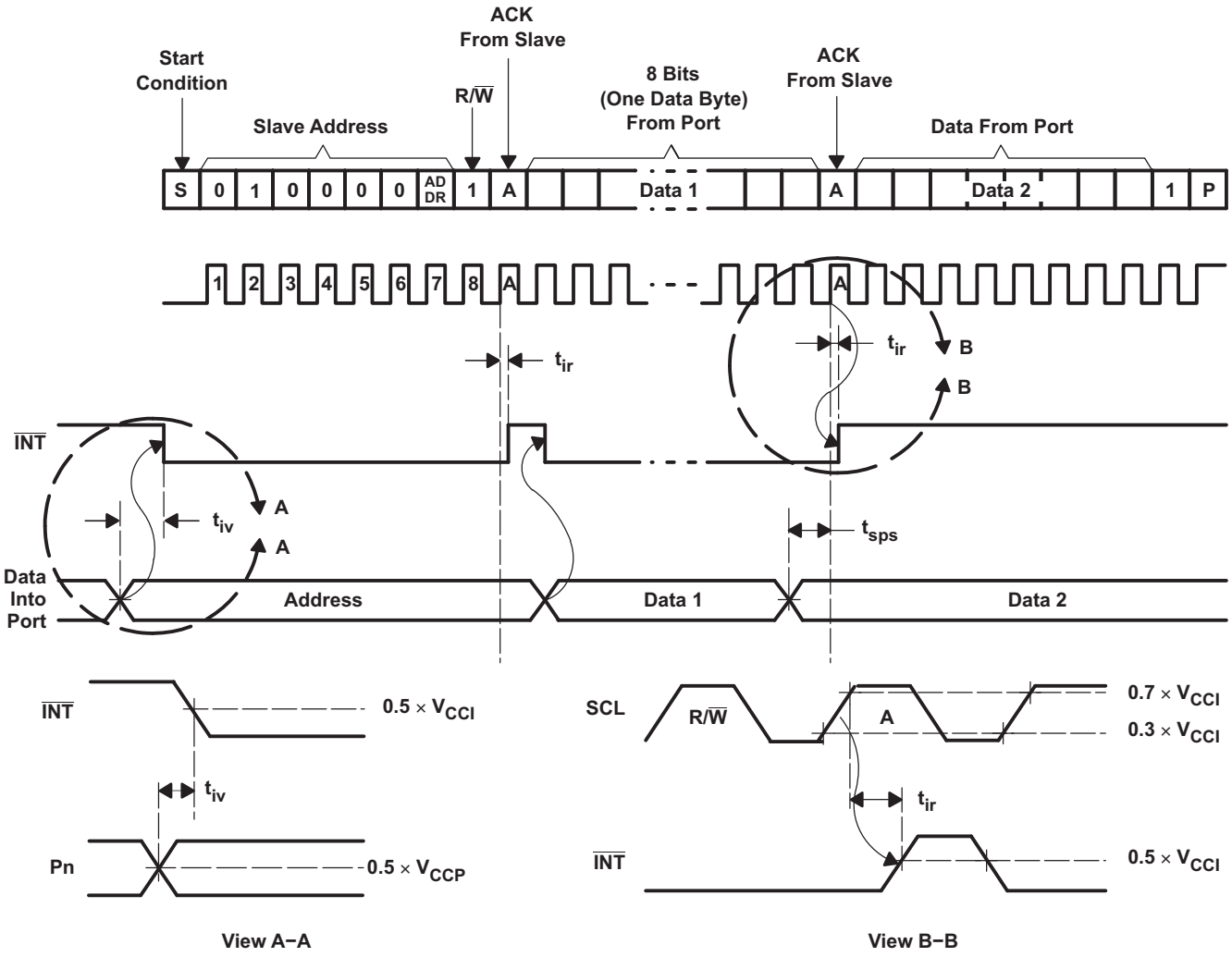
C. All parameters and waveforms are not applicable to all devices.

Figure 13. I^2C Interface Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)



INTERRUPT LOAD CONFIGURATION



View A–A View B–B

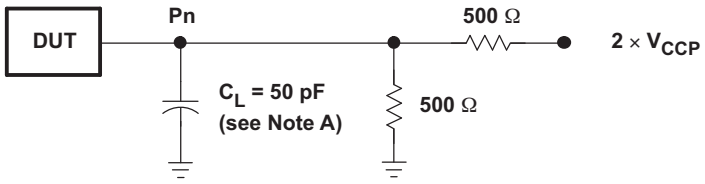
A. C_L includes probe and jig capacitance.

B. All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f ≤ 30 ns.

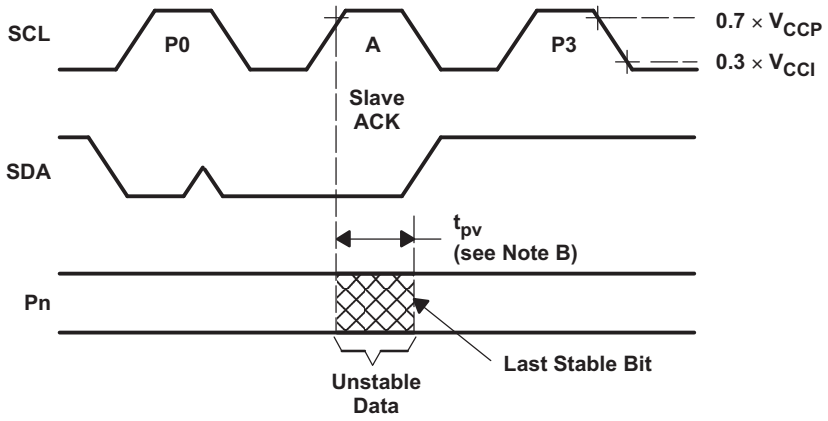
C. All parameters and waveforms are not applicable to all devices.

Figure 14. Interrupt Load Circuit and Voltage Waveforms

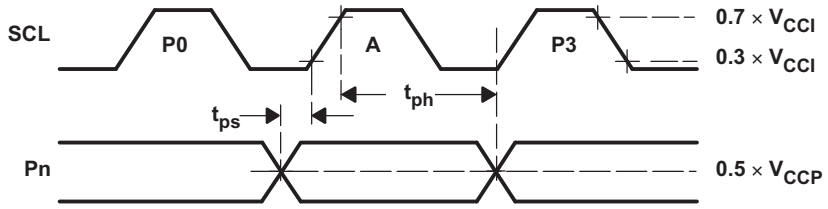
PARAMETER MEASUREMENT INFORMATION (continued)



P-PORT LOAD CONFIGURATION



WRITE MODE (R/$\overline{W}$ = 0)



READ MODE (R/$\overline{W}$ = 1)

A. C_L includes probe and jig capacitance.

B. t_{pv} is measured from 0.7 × V_{CC} on SCL to 50% I/O (Pn) output.

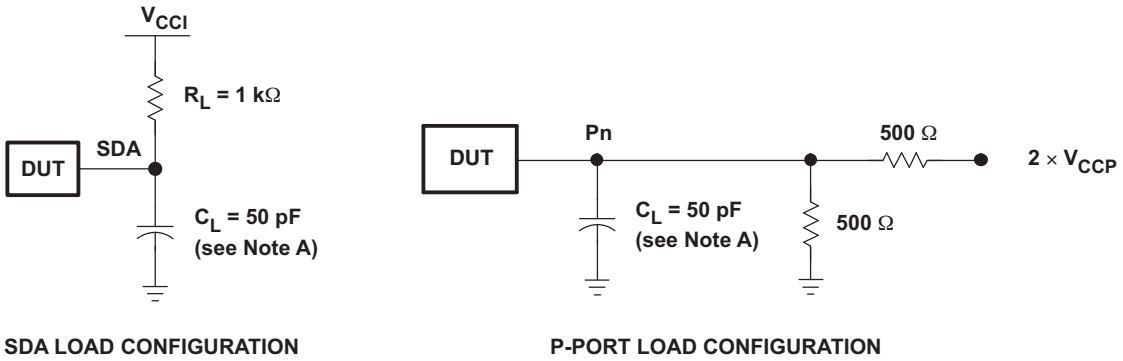
C. All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f ≤ 30 ns.

D. The outputs are measured one at a time, with one transition per measurement.

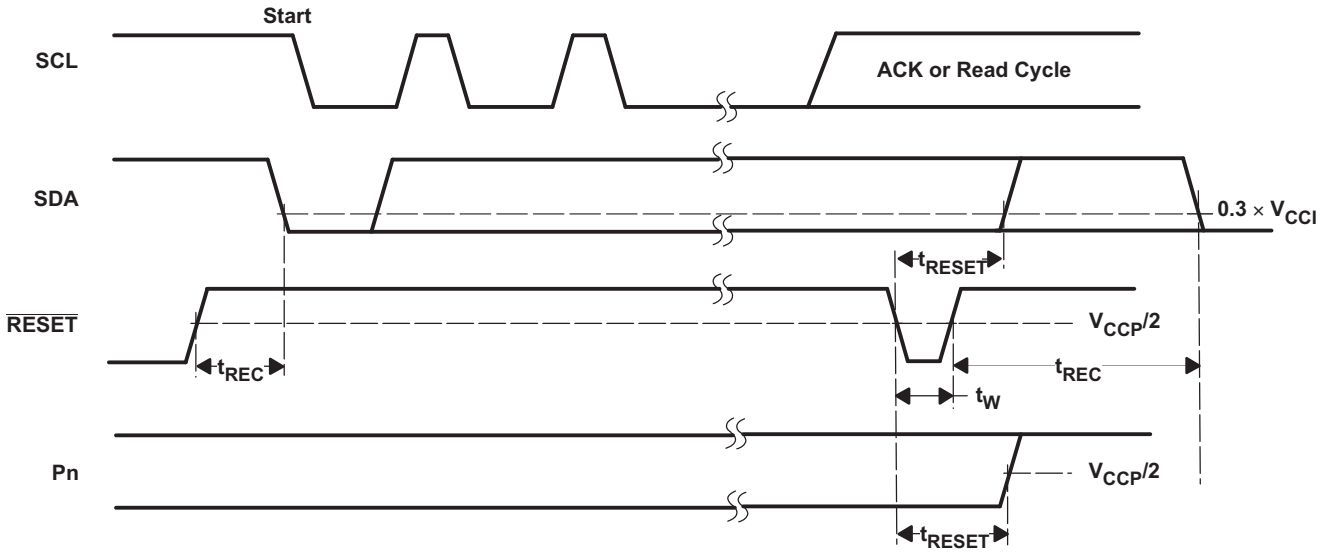
E. All parameters and waveforms are not applicable to all devices.

Figure 15. P Port Load Circuit and Timing Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)



SDA LOAD CONFIGURATION P-PORT LOAD CONFIGURATION



A. C_L includes probe and jig capacitance.
B. All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f ≤ 30 ns.
C. The outputs are measured one at a time, with one transition per measurement.
D. I/Os are configured as inputs.
E. All parameters and waveforms are not applicable to all devices.

Figure 16. Reset Load Circuits and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TCA8418RTWR	ACTIVE	QFN	RTW	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

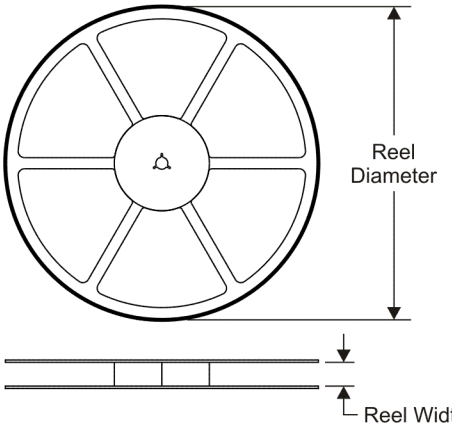
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

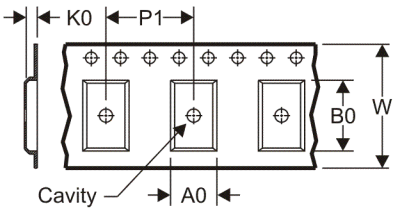
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

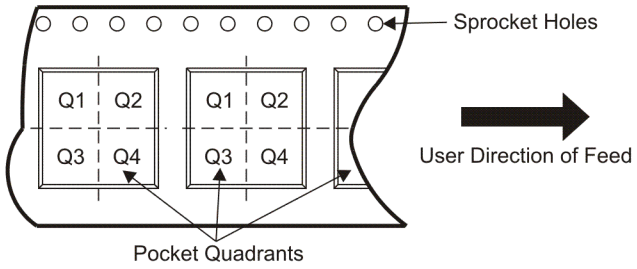


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

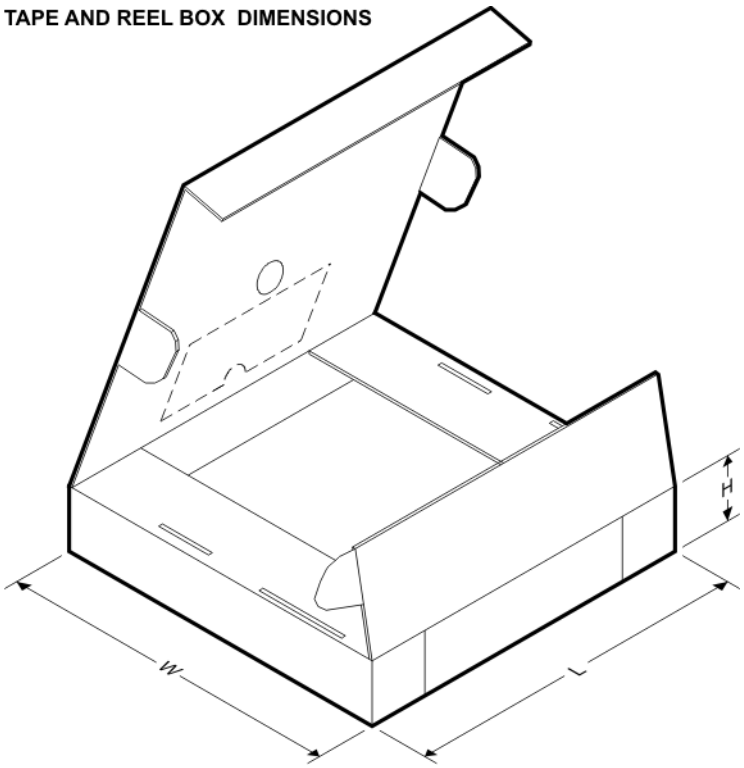
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TCA8418RTWR	QFN	RTW	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

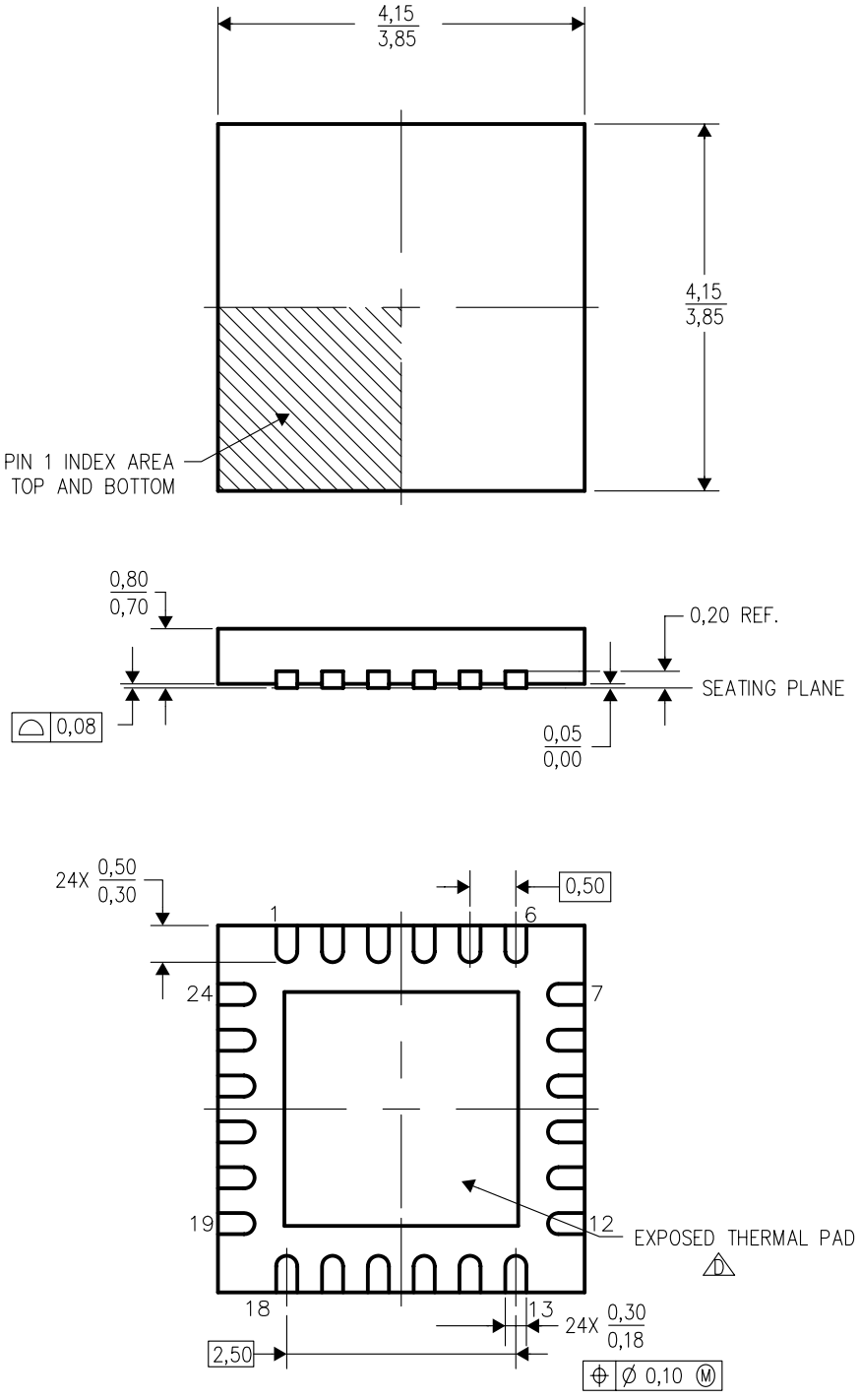
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TCA8418RTWR	QFN	RTW	24	3000	346.0	346.0	29.0

RTW (S–PQFP–N24) PLASTIC QUAD FLATPACK



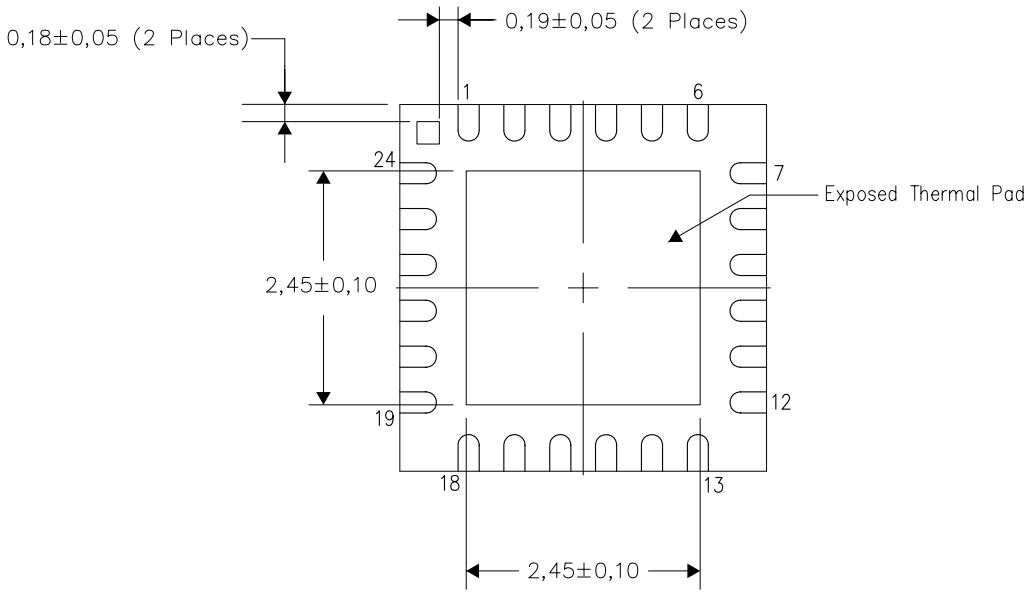
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–Leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–220.

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

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