

# TOSHIBA MOS MEMORY PRODUCTS

256K BIT (32K WORD × 8 BIT) MASK ROM  
N-CHANNEL SILICON GATE

TMM23256P

020468

## DESCRIPTION

The TMM23256P is a 262,144 bit read only memory organized as 32,768 words by 8 bits with a low bit cost, thus being most suitable for use in character generator.

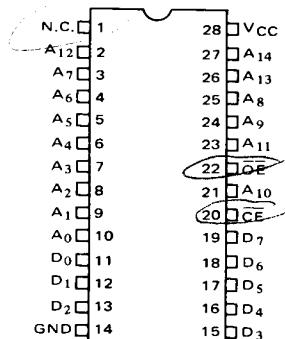
Consisting of static memory cells and clocked peripheral circuitry, the TMM23256P provides a high speed and low power dissipation (access time 150ns, operating current 40mA).

The TMM23256P also features an automatic stand-by power mode. When deselected by Chip Enable ( $\overline{CE}$ ), the operating current is reduced from 40mA to

## FEATURES

- Single 5V Power Supply
- Fast Access Time : 150ns (Max.)
- Low Power Dissipation
  - Average Current : 40mA (Max.)
  - Standby Current : 10mA (Max.)
- Inputs protected : All Inputs have Protection Against Static Charge

## PIN CONNECTION



## PIN NAMES

$A_0 \sim A_{14}$	Address Inputs
$D_0 \sim D_7$	Data Outputs
$OE$	Output Enable Input
$CE$	Chip Enable Input
N.C.	No Connection
Vcc	Power Supply Terminal
GND	Ground

10mA. Output Enable ( $\overline{OE}$ ) is effective in preventing data confliction on a common bys line.

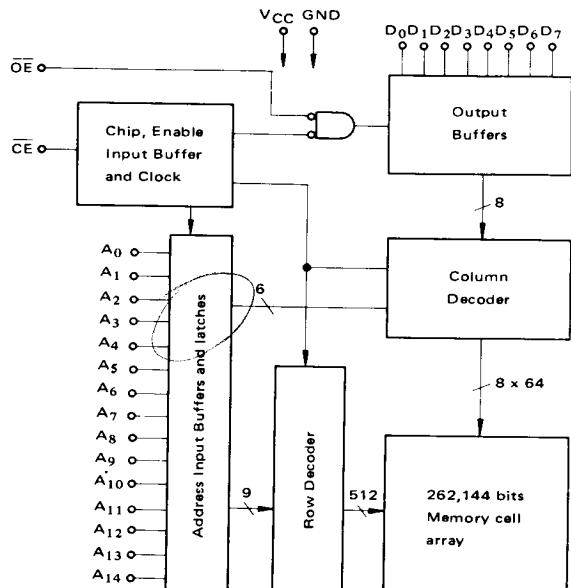
The TMM23256P uses the address latch system that the falling edge of  $\overline{CE}$  latches all inputs except for  $\overline{OE}$ , thus can be easily connected to a system where address and data buses are commonly used.

The TMM23256P is fabricated with ion implanted N-channel silicon gate technology. This technology allows a production on high performance.

The TMM23256P is moulded in a 28 pin standard plastic package, 0.6 inch in width.

- Edge Enabled Operation :  $CE$
- Output Buffer Control :  $OE$
- Input and Output : TTL Compatible
- Three State Outputs : Wired OR Capability
- 28 pin Standard Plastic DIP

## BLOCK DIAGRAM



# TMM23256P

## MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V <sub>CC</sub>	Power Supply Voltage	-0.5 ~ 7.0	V
V <sub>IN</sub> , V <sub>OUT</sub>	Input and Output Voltage	-0.5 ~ 7.0	V
T <sub>OPR</sub>	Operating Temperature	0 ~ 70	°C
T <sub>STRG</sub>	Storage Temperature	-55 ~ 150	°C
T <sub>SOLDER</sub>	Soldering Temperature · Time	260 · 10	°C · sec
P <sub>D</sub>	Power Dissipation (Ta = 70°C)	1.0	W

## D.C. OPERATING CONDITIONS (Ta = 0 ~ 70°C)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V <sub>IH</sub>	Input High Voltage	-	2.2	-	V <sub>CC</sub> + 1	V
V <sub>IL</sub>	Input Low Voltage	-	-0.5	-	0.8	V
V <sub>CC</sub>	Power Supply Voltage	-	4.5	5.0	5.5	V

## D.C. and OPERATING CHARACTERISTICS (Ta = 0 ~ 70°C)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I <sub>IH</sub>	Input High Current	V <sub>IN</sub> = 5.5V	-	0.05	10	μA
I <sub>IL</sub>	Input Low Current	V <sub>IN</sub> = GND	-	-0.05	-10	μA
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -400μA	2.4	3.3	-	V
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = 3.2mA	-	0.3	0.4	V
I <sub>LOH</sub>	Output Leakage Current	V <sub>OUT</sub> = 5.5V	-	0.05	10	μA
I <sub>LOL</sub>		V <sub>OUT</sub> = 0.4V	-	-0.1	-20	μA
I <sub>CC1</sub>	Standby Current	CE = 2.2V	-	-	10	mA
I <sub>CC2</sub>	Average Current	t <sub>CYC</sub> = 230ns, I <sub>OUT</sub> = 0mA	-	-	40	mA

- Typical values are at Ta = 25°C and V<sub>CC</sub> = 5V.

## CAPACITANCE (Ta = 25°C, f = 1MHz)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = A.C. GND	-	5	10	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = A.C. GND	-	8	15	pF

Note : This parameter is periodically sampled and is not 100% tested.

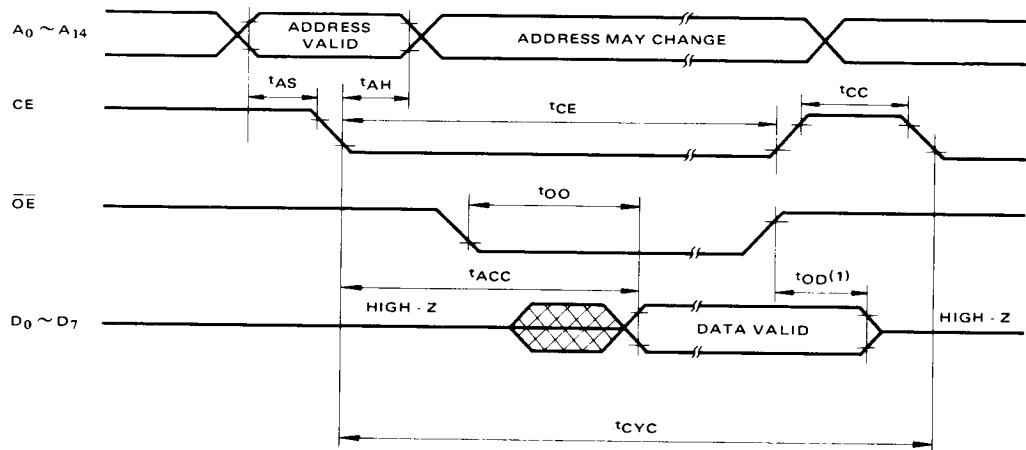
**A.C. CHARACTERISTICS**(Ta = 0 ~ 70°C, V<sub>CC</sub> = 5V ± 10%)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t <sub>CE</sub>	CE pulse width	—	150	—	—	ns
t <sub>AS</sub>	Address Setup Time	—	0	—	—	ns
t <sub>AH</sub>	Address Hold Time	—	30	—	—	ns
t <sub>ACC</sub>	Access Time	—	—	—	150	ns
t <sub>OO</sub>	Output Delay Time from OE	—	—	—	70	ns
t <sub>OD</sub>	Output Turn off Delay	—	—	—	70	ns
t <sub>CC</sub>	CE off Time	—	70	—	—	ns
t <sub>CYC</sub>	Cycle Time	t <sub>AS</sub> = 0ns, t <sub>r</sub> , t <sub>f</sub> = 5ns	230	—	—	ns

- Typical values are at Ta = 25°C and V<sub>CC</sub> = 5V.

**A.C. TEST CONDITIONS**

- Output Load : 1 TTL Gate + 100pF
- Input Rise and Fall Times (10% ~ 90%) : 5ns
- Input Pulse Levels : 0.8 ~ 2.4V
- Timing Measurement Reference Levels : Input ; 1V and 2.2V  
Output ; 0.8V and 2.0V

**TIMING WAVEFORMS**

Note (1) t<sub>OD</sub> is specified from OE or CE, whichever occurs first.

# TMM23256P

## OPERATION INFORMATION

The TMM23256P has two control functions.

The chip enable ( $\overline{CE}$ ) controls the operation power and should be used for device selection. The falling edge of the  $\overline{CE}$  will activate the device and latch the addresses. The output enable ( $\overline{OE}$ ) control the out-

put buffers, independent of device selection. Assuming that  $\overline{OE} = V_{IL}$ , the output data is valid at the outputs after  $t_{ACC}$  (150ns) from the falling edge of the  $\overline{CE}$ .

The operation modes of the TMM23256P are listed in the following table.

MODE	$\overline{CE}$	ADDRESS	$\overline{OE}$	OUTPUT	POWER
Standby	H	*	*	High Impedance	Standby
Latch	L	Valid	*	High Impedance	-
Read	L	**	L	Data Out	Active
Output Deselect	L	*	H	High Impedance	Active

Note \* : Don't care

\*\* : Address may change after  $t_{AH}$ .

**APPLICATION INFORMATION****1. POWER SUPPLY DECOUPLING**

The operating current  $I_{CC}$  waveforms for TMM23256P are shown in Fig. 1, 2.

The TMM23256P is a clocked device, so the transient current peaks are produced on the  $\overline{CE}$  transition and  $\overline{CE}$  active level.

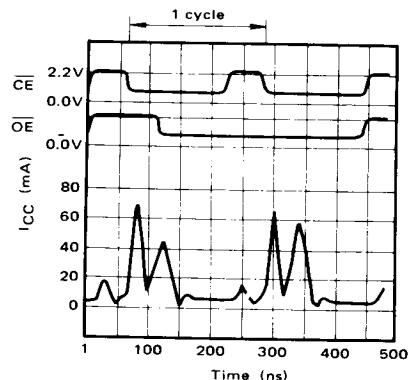
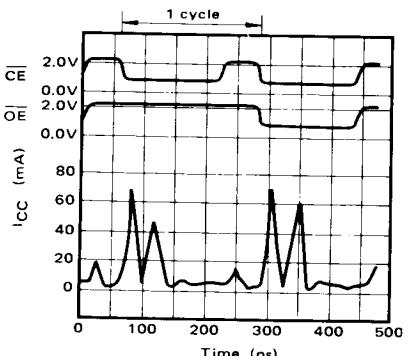
The  $I_{CC}$  current transients require adequate decoupling of  $V_{CC}$  power supply.

**2. POWER ON**

The TMM23256P requires initialization prior to normal operation. Two initialization methods are as follows:

- (1) A minimum  $100\mu s$  time delay is required after the application of  $V_{CC}$  (+5V) before proper device operation is achieved. And during this period,  $\overline{CE}$  must be at  $V_{IH}$  level.
- (2) A minimum  $100\mu s$  time delay is required after the application of  $V_{CC}$  (5V), and then a minimum of one initialization cycle must be performed before proper device operation is achieved.

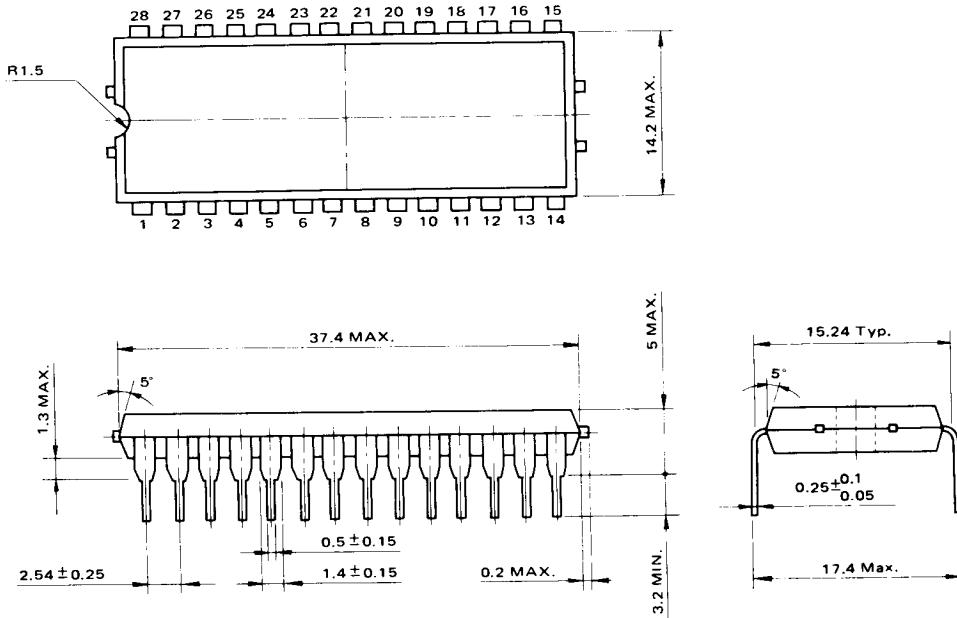
Initialization cycle : An initialization cycle is one Chip Enable clock cycle from the first down edge of the  $\overline{CE}$  till the next down edge.

Fig. 1  $I_{CC}$  vs. Time (1)Fig. 2  $I_{CC}$  vs. Time (2)

# TMM23256P

## OUTLINE DRAWINGS

Unit : mm



Note : Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect to No.1 and No.28 leads.