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■ MB831124-35
1M-BIT (131,072×8) CMOS
## Read Only Memory

Description

The Fujitsu MB831124 is a CMOS Si-gate mask-programmable static read only memory organized as 131,072 words by 8 bits.

The MB831124 has TTL-compatible I/O and 3-state output level with $\overline{CE}$ clocked operation and single +5V power supply. The MB831124 is designed for applications such as character generator or program storage which require large memory capacity, high-speed and low power operation.

The package for the MB831124 is a standard 28-pin dual-in-line package.

Features

- **Organization:**
  131,072 words × 8 bits
- **Fast access time:**
  350 ns max. (MB831124-35)
- **Fast cycle time:**
  460 ns max. (MB831124-35)
- **Clocked control ($\overline{CE}$) periphery**
- **TTL compatible inputs/ outputs**
- **Three-state outputs**

- **Single +5V supply, ±10% tolerance**
- **Power consumption:**
  138 mW (Operation)
  5.5 mW (Standby, TTL input level)
  0.165 mW (Standby, CMOS input level)
- **Standard 28-pin DIP**
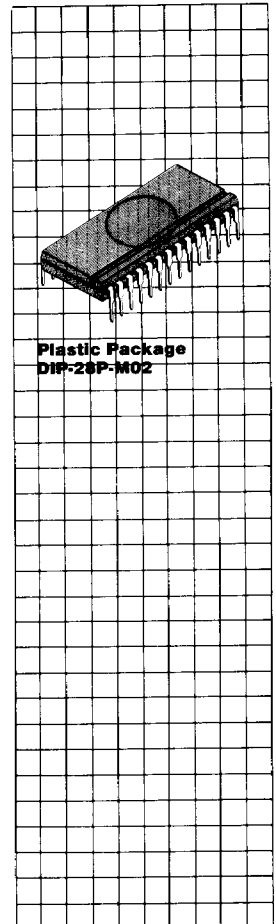
**Plastic Package
DIP-28P-M02**

MB831124
Block Diagram
and Pin Assignment
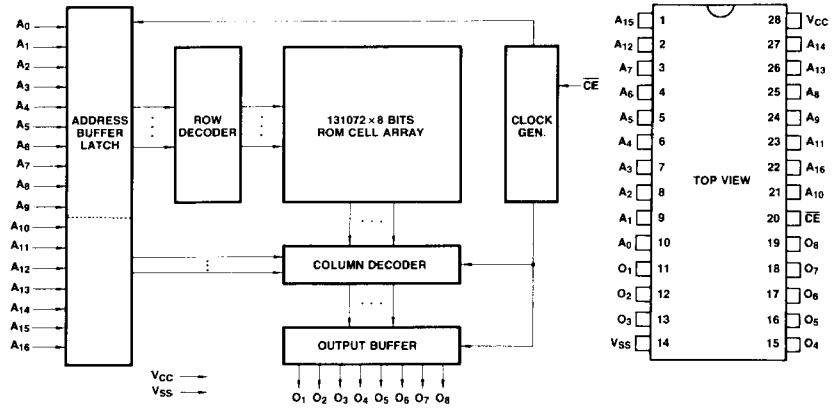
Absolute Maximum Ratings
(See Note)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to $+0.7$	V
Input Voltage on Any Pin with respect to GND	V_{IN}	-0.5 to $V_{CC} + 0.5$	V
Output Voltage on Any Pin with respect to GND	V_{OUT}	-0.5 to $V_{CC}+0.5$	V
Temperature under Bias	T_{BIAS}	-10 to $+85$	°C
Storage Temperature	T_{STG}	-45 to $+125$	°C

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating
Conditions
(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Low Voltage	V_{IL}	-0.3		0.8	V
Input High Voltage	V_{IH}	2.2		$V_{CC}+0.3$	V
Ambient Temperature	T_A	0		70	°C

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Capacitance
(T_A = 25°C, f = MHz)

| Parameter	Symbol	Typ	Max	Unit
Input Capacitance (V_{IN} = 0 V)	C_{IN}		10	pF
Output Capacitance (V_{OUT} = 0 V)	C_{OUT}		15	pF

DC Characteristics
(Recommended operating conditions unless otherwise noted.)

Parameter	Test Condition	Symbol	Min	Max	Unit
Input Leakage Current	V_{IN} = 0 V to V_{CC}	I_{LI}	−10	10	μA
Output Leakage Current	$\overline{CE}$ = V_{IH}, V_{OUT} = 0 V to V_{CC}	I_{LO}	−10	10	μA
Active Supply Current	t_{CYC} = 460 ns, t_{CE} = 350 ns	I_{CC1}		25	mA
Standby Supply Current	$\overline{CE}$ = V_{IH}	I_{SB1}		1	mA
Standby Supply Current	V_{CC} −0.2 ≤ CE ≤ V_{CC} +0.2	I_{SB2}		30	μA
Output Low Voltage	I_{OL} = 2.1 mA	V_{OL}		0.4	V
Output High Voltage	I_{OH} = −400 μA	V_{OH}	2.4		V

AC Characteristics
(Recommended operating conditions unless otherwise noted.)

Parameters	Symbol	MB831124-35		Unit	Conditions
		Min	Max		
Cycle Time	t_{CYC}	460		ns	
Chip Enable Pulse Width	t_{CE}	350		ns	
Address Access Time	t_{ACC}		350	ns	
Output Disable Time	t_{OFF}		80	ns	t_{CYC} = t_{CE} + t_{CC} + $2t_T$ t_T = 5 ns
Address Setup Time	t_{AS}	0		ns	
Address Hold Time	t_{AH}	80		ns	
Chip Enable Off Time	t_{CC}	100		ns	

Timing Diagram
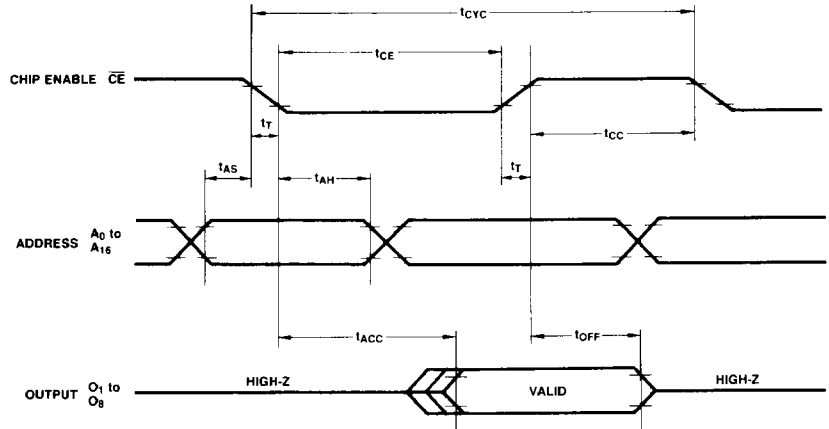
AC Test Conditions

Input Pulse Levels: 0.6 to 2.4 V
Input Pulse Rise and Fall Times: 5 ns
Timing Reference Levels: Input: $V_{IL} = 0.8$ V, $V_{IH} = 2.2$ V
Output: $V_{OL} = 0.8$ V, $V_{OH} = 2.2$ V
Output Load: 1 TTL Gate and $C_L = 100$ pF
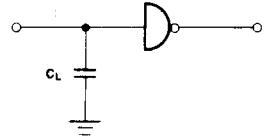
MB831124 ROM Code Data Input Method

Mask ROM Code Data Release by EPROMs:

128K EPROM:

When the customer releases his Mask ROM Data in the form of EPROMs, he should use eight MBM27128 or equivalent and program data of 8 address blocks (Address 0 to 16 K, 16 K to 32 K, 32 K to 48 K, 48 K to 64 K, 64 K to 80 K, 80 K to 96 K, 96 K to 112 K and 112 K to 128 K) of the MB831124 to each MBM27128 EPROM. Fujitsu requires 3 sets, total 24 pcs, of such programmed EPROMs. (Two sets, total 16 pcs, are acceptable.)

In addition to the programmed sets, Fujitsu requires an additional set of blank EPROMs (8 pcs) for supplying customer ROM Data Code verification.

MSB																LSB
A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	0	0	MBM27128 (No. 1: 0 to 16 K)													
0	0	1	MBM27128 (No. 2: 16 K to 32 K)													
0	1	0	MBM27128 (No. 3: 32 K to 48 K)													
0	1	1	MBM27128 (No. 4: 48 K to 64 K)													
1	0	0	MBM27128 (No. 5: 64 K to 80 K)													
1	0	1	MBM27128 (No. 6: 80 K to 96 K)													
1	1	0	MBM27128 (No. 7: 96 K to 112 K)													
1	1	1	MBM27128 (No. 8: 112 K to 128 K)													

256K EPROM:

When the customer releases his Mask ROM Data in the form of EPROMs, he should use four MBM27C256 or equivalent and program data of 4 address blocks (Address 0 to 32 K, 32 K to 64 K, 64 K to 96 K and 96 K to 128 K) of the MB831124 to each MBM27C256 EPROM.

Fujitsu requires 3 sets, total 12 pcs, of such programmed EPROMs. (Two sets, total 8 pcs, are acceptable.)

In addition to the programmed sets, Fujitsu requires an additional set of blank EPROMs (4 pcs) for supplying customer ROM Data Code verification.

MSB   LSB

A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	0									MBM27C256 (No. 1: 0 to 32 K)						
0	1									MBM27C256 (No. 2: 32 K to 64 K)						
1	0									MBM27C256 (No. 3: 64 K to 96 K)						
1	1									MBM27C256 (No. 4: 96 K to 128 K)						

**Mask ROM Code Data Release by Magnetic Tapes:**

When the customer releases his Mask ROM Code Data in the form of Magnetic Tapes (MT), he should use tapes that can be used on IBM compatible equipment and meet the following requirements.

■ Physical Requirements:
1 Length: 2400 feet, 1200 feet, or 600 feet
2 Width: ½ inch
3 Track: 9 tracks
4 Density: 800 BPI or 1600 BPI

■ MT Format:
1 Label: No tape mark on the header of tape
2 Record Size: 80 bytes/ record
3 Block Size: Single record/ block
4 File: Single file/volume
5 Code Used: EBCDIC code
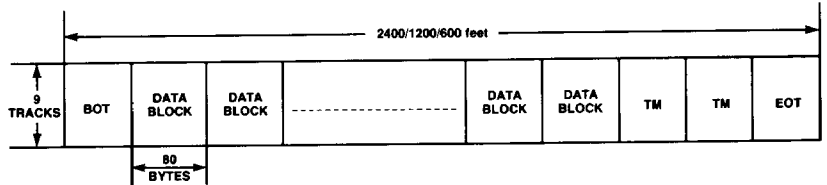
NOTE: BOT : BEGINNING OF TAPE
EOT : END OF TAPE
TM : TAPE MARK

■ Data Block Format:

ROW NUMBER	1 ⎯ 9	10 ⎯ 15	16 ⎯ 19	20 ⎯ 67	68 ⎯ 72	73 ⎯ 80

UNDEFINED FIELD	ADDRESS FIELD (1 HEAD ADDRESS)	UNDEFINED FIELD	DATA FIELD (16 WORDS)	UNDEFINED FIELD	SEQUENCE
NUMBER OF BYTE: 9 BYTES	6 BYTES	4 BYTES	48 BYTES	5 BYTES	8 BYTES

NOTE: 1 BYTE/ROW

Undefined Field (Row 1~9/ Row 16~19/Row 68~72):

In this field, blanks (∅) should be recorded.

Address Field (Row 10~15):

In the address field, the header address of the 16-word data that follows the address field should be recorded in the form of a five-digit hexadecimal number following a symbol "#". The corresponding binary address to this hex address is shown in the following example.

	MSB																LSB
ADDRESS BIT	A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
BINARY ADDRESS	0	0	0	1	1	1	0	1	1	1	0	0	1	0	0	1	0
HEX ADDRESS	0		3			8				9				2			
RECORDED FORM	#03B92																

Data Field (Row 20~67):

In this field, 16-word data with 16 successive addresses should be recorded in the form of two-digit hexadecimal numbers followed by a blank (∅). (The header data is for the address recorded in the address field.) The corresponding binary data to this hex data is shown in the following example.

DATA BIT	08	07	06	05	04	03	02	01
BINARY DATA	1	1	1	1	0	0	1	0
HEX DATA			F				2	
RECORDED DATA	F2∅							

Sequence Number Field (Row 73~80):

In this field, the sequence number of each record (data block) should be recorded in the form of an eight-digit decimal number, which must be counted up by tens. All digits to the left of the most significant digit should be zeros, not blanks. Refer to the following example.

ADDRESS		DATA					SEQUENCE NO.	
10	15	20	22	23	25	65	67	73	80
#03B92		F2∅		A0∅		- -	07∅	00000010	

Package Dimensions

Dimensions in
inches (millimeters)

28-Lead Plastic Dual In-Line Package (Case No.: DIP-28P-M02)