

Bipolar Memories

FUJITSU

■ MB7117E/H, MB7118E/H Schottky TTL 2048-Bit Bipolar Programmable Read-Only Memory

Description

The Fujitsu MB7117 and MB7118 are high speed Schottky TTL electrically field programmable read only memories organized as 256 words by 8-bits. With uncommitted collector outputs provided on the MB7117 and three-state outputs on the MB7118 memory expansion is simple.

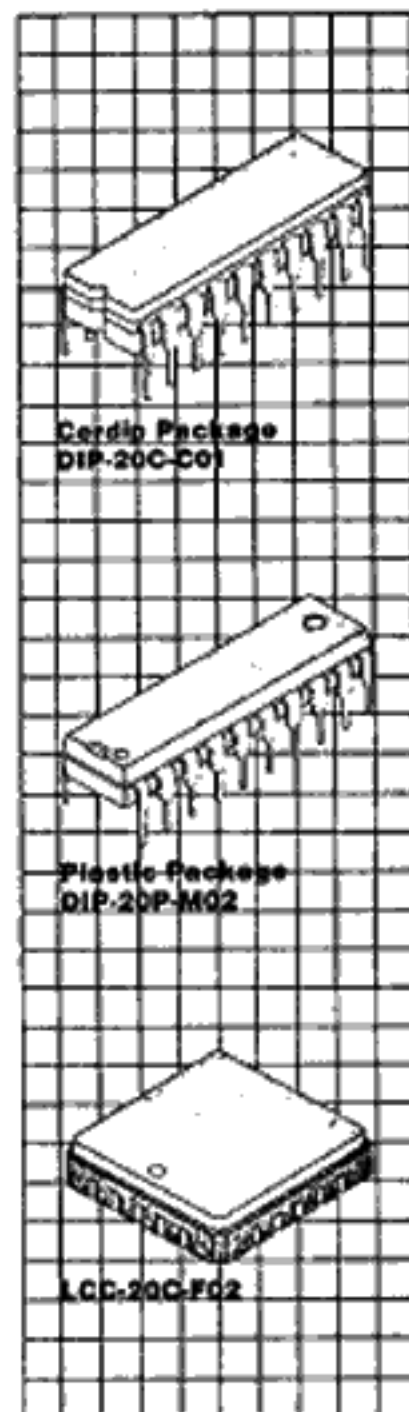
The memory is fabricated with all logic "zeros" (positive logic). Logic level "ones" can be programmed by the highly reliable DEAP™ (Diffused Eutectic Aluminum Process) according to simple programming procedures.

The sophisticated passive isolation termed IOP (Isolation by Oxide and Polysilicon) with thin epitaxial layer and Schottky TTL process permits minimal chip size and fast access time.

Extra test cells and unique testing methods provide enhanced correlation between programmed and unprogrammed circuits in order to perform AC, DC and programming test prior to shipment. This results in extremely high programmability.

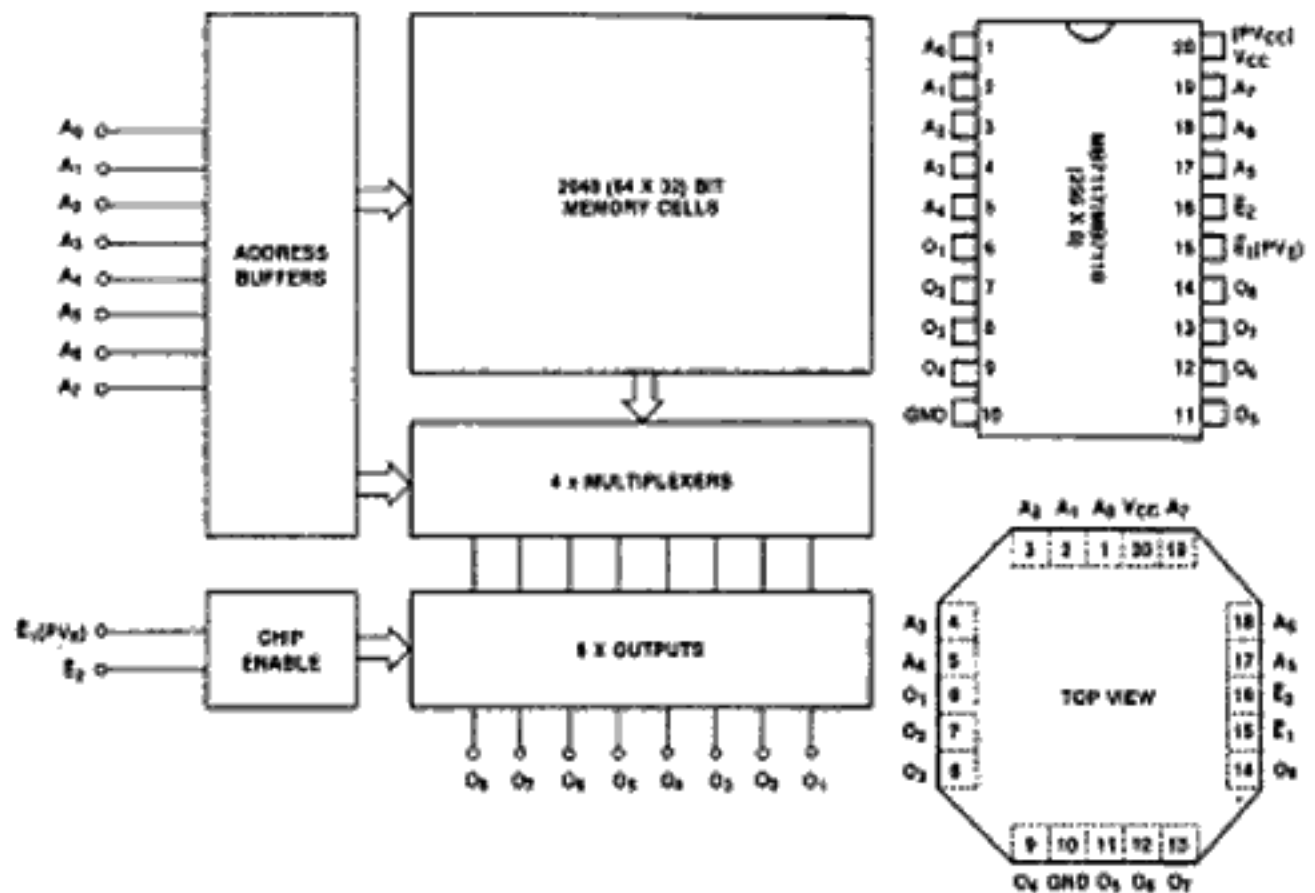
Features

- Single +5V supply voltage
- Organized as 256 words by 8-bits, fully decoded
- Proven higher programmability and reliability
- Programming by DEAP™ (Diffused Eutectic Aluminum Process)
- Simplified, low power programming
- Low current PNP inputs
- AC characteristics guaranteed over full operating voltage and temperature range via unique testing techniques
- Fast access time, 26 nsec typ.
E—45 nsec max.
H—35 nsec max.
- TTL compatible inputs and outputs
- Open collector outputs, MB7117
- Three-state outputs, MB7118
- Two chip enables for simplified memory expansion
- Standard 20-pin DIP package
- JEDEC approved pin out



MB7117E/H
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Block Diagram and Pin Assignment



Absolute Maximum Ratings
(See Note)

Rating	Symbol	Value	Unit
Power supply voltage	V_{CC}	-0.5 to +7.0	V
Power supply voltage (during programming)	V_{CC}	-0.5 to +7.5	V
Input voltage	V_{IN}	-1.5 to +5.5	V
Input voltage (during programming)	V_{PRG}	22.5	V
Output voltage (during programming)	V_{PRG}	0.5 to +22.5	V
Input current	I_{IN}	-20	mA
Input current (during programming)	I_{PRG}	+270	mA
Output current	I_{OUT}	+100	mA
Output current (during Programming)	I_{PRG}	+150	mA
Storage temperature	Ceramic Plastic	T_{STG} -65 to +150 -40 to +125	$^{\circ}C$
Output voltage	V_{OUT}	-0.5 to V_{CC}	V

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to conditions as detailed in the operational sections of this data sheet. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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Guaranteed Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.0	5.25	V
Input low voltage	V_{IL}	0		0.8	V
Input high voltage	V_{IH}	2.0		5.5	V
Ambient temperature	T_A	0		75	°C

Capacitance

($f = 1\text{MHz}$, $V_{CC} = +5\text{V}$,
 $V_{IN} = +2\text{V}$, $T_A = 25^\circ\text{C}$)

Parameter	Symbol	Min	Typ	Max	Unit
input capacitance	C_I			10	pF
Output capacitance	C_O			12	pF

DC Characteristics

(Full guaranteed operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit
Input leakage current ($V_{IH} = 5.5\text{V}$)	I_{IL}			40	μA
Input load current ($V_{IL} = 0.45\text{V}$)	I_I			-250	μA
Output low voltage ($I_{OL} = 10\text{mA}$)	V_{OL}			0.45	V
Output low voltage ($I_{OL} = 16\text{mA}$)	V_{OL}			0.50	V
Output leakage current ($V_O = 2.4\text{V}$, chip disabled)	MB7117 I_{OLK}			40	μA
Output leakage current ($V_O = 2.4\text{V}$, chip disabled)	MB7118 I_{OLH}			40	μA
Output leakage current ($V_O = 0.45\text{V}$, chip disabled)	MB7118 I_{OLE}			-40	μA
Input clamp voltage ($I_{IN} = -18\text{mA}$)	V_{IC}			-1.2	V
Power supply current ($V_{IN} = \text{OPEN or GND}$)	I_{CC}		80	140	mA
Output high voltage ($I_O = -2.4\text{mA}$)	MB7118 V_{OH}^{*1}	2.4			V
Output short circuit current ($V_O = \text{GND}$)	MB7118 I_{OS}^{*1}	-15		-60	mA

Note: *1 Denotes guaranteed characteristics of the output high level (OH) state when the chip is enabled ($V_{CE} = 2.4\text{V}$) and the programmed bit is addressed. These characteristics cannot be tested prior to programming, but are guaranteed by factory testing.

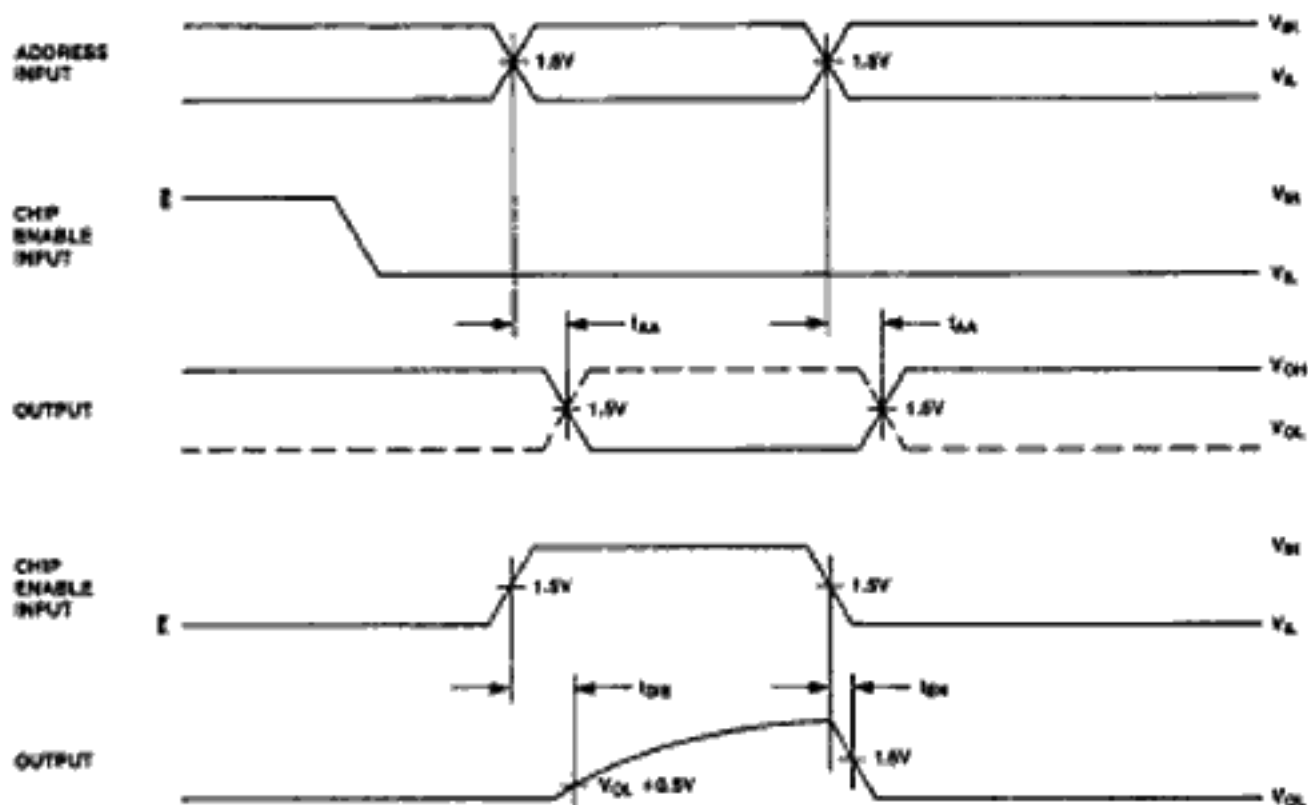
AC Characteristics

(Full guaranteed operating conditions unless otherwise noted.)

Parameter	Symbol	MB7117E/ MB7118E		MB7117H/ MB7118H		Unit
		Typ	Max	Typ	Max	
Access time (via address input)	t_{AA}	25	45	25	35	ns
Output disable time	t_{OD}		30		30	ns
Output enable time	t_{EN}		30		30	ns

MB7117E/H
MB7118E/H

Operation Timing Diagram

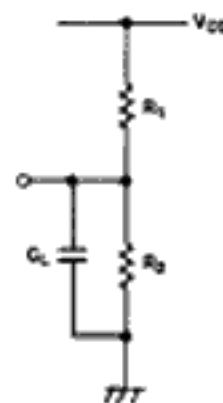


NOTE: OUTPUT DISABLE TIME IS THE TIME TAKEN FOR THE OUTPUT TO REACH A HIGH RESISTANCE STATE WHEN THE CHIP ENABLE IS TAKEN HIGH (DISABLED). OUTPUT ENABLE TIME IS THE TIME TAKEN FOR THE OUTPUT TO BECOME ACTIVE WHEN ALL OF CHIP ENABLES ARE TAKEN LOW (ENABLED). THE HIGH RESISTANCE STATE IS DEFINED AS A POINT ON THE OUTPUT WAVEFORM EQUAL TO A 1V OF 0.5V FROM THE ACTIVE OUTPUT LEVEL.

AC Test Conditions

Input Conditions
Amplitude: 0V to 3V
Rise and Fall Time: 5 ns from 1V to 2V
Frequency: 1MHz

	R_1	R_2	C_L
t_{AA}	300 Ω	600 Ω	30pF
t_{OE}	300 Ω	600 Ω	30pF
t_{ON}	300 Ω	600 Ω	30pF



MB7117E/H
MB7118E/H

Input/Output Circuit Information

Input Circuit

Schottky TTL circuit technology is used in the input circuit to achieve high-speed operation. A PNP transistor in the first stage of the input circuit improves input high/low current characteristics remarkably. The input circuit also includes a protection diode for reliable operation.

Open Collector Output

The open collector output is often utilized in high-speed applications where power dissipation must be minimized. When the device is switched, there is no current sourced from the supply rail. Consequently, the current spike normally associated with TTL totem-pole outputs is eliminated. In high-frequency applications, this minimizes noise problems (false triggering) as well as power drain. For example, the transient current (low impedance high-level to low impedance low-level) is typically 30mA for the MB7118 (three-state) compared to 0mA for the MB7117 (open-collector).

Three-State Output

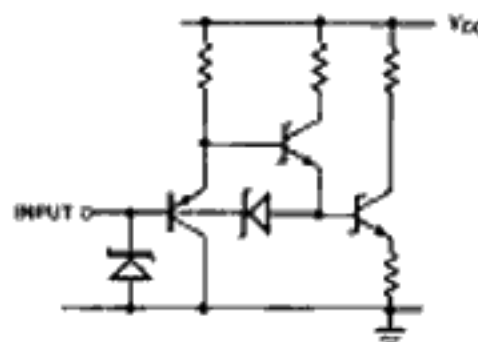
A "three-state" output is a logic element which has three distinct output states of ZERO, ONE and OFF (wherein OFF represents a high-impedance condition which can neither sink nor source current at a definable logic level). Effectively, then, the device has all the desirable features of a totem-pole TTL output (e.g., greater noise immunity, good rise time, line driving capacity), plus the ability to connect to bus-organized systems.

In the case where two devices are on at the same time, the possibility exists that they may be in opposite (one a ONE and one a ZERO) impedance states simultaneously; thus, the short circuit current from one enabled device may flow through the other enabled device. While physical damage under these conditions is unlikely, system noise problems could result. Therefore, the system designer should consider these factors to ensure that this condition does not exist.

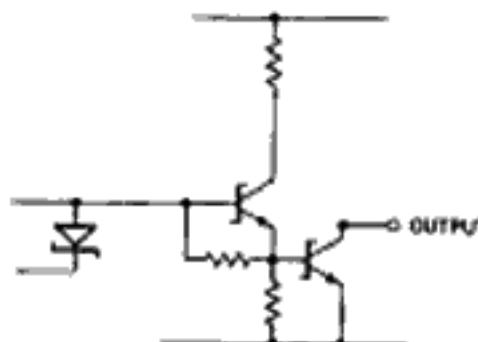
Also in the output circuit, Schottky TTL circuit technology is used to achieve high-speed operation. A PNP transistor is

also provided in the output circuit and is effective in decreasing a load for the Chip Enable circuit.

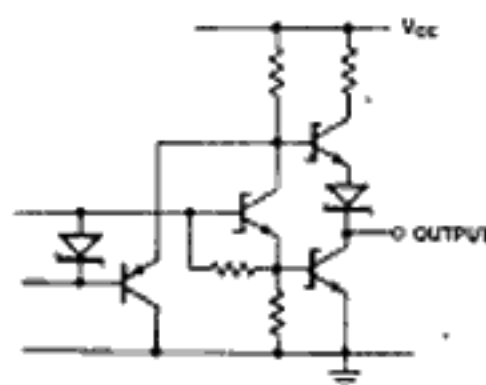
MB7117/MB7118 Input Circuit



MB7117 Output Circuit



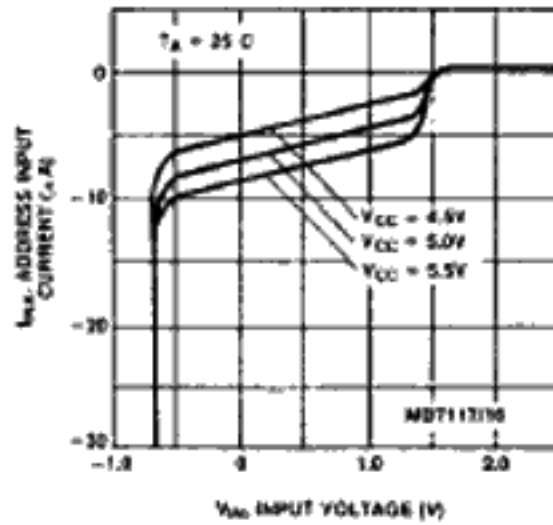
MB7118 Output Circuit



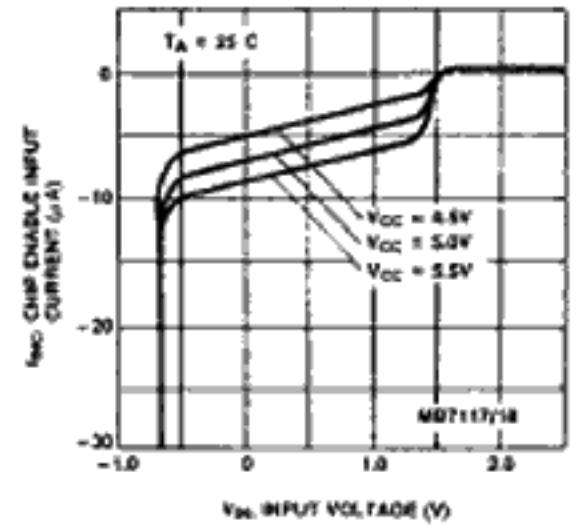
MB7117E/H
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Typical Characteristics Curves

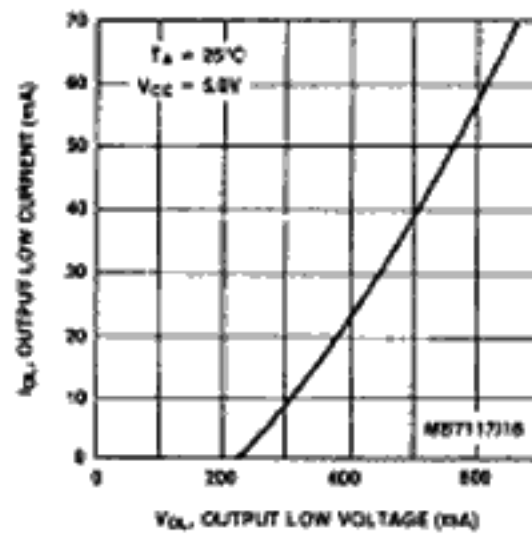
I_{INA} Input Current vs. V_{IN} Input Voltage



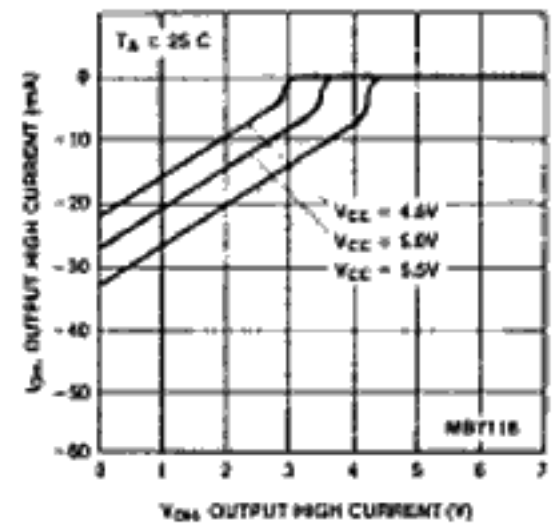
I_{INC} Input Current vs. V_{IN} Input Voltage



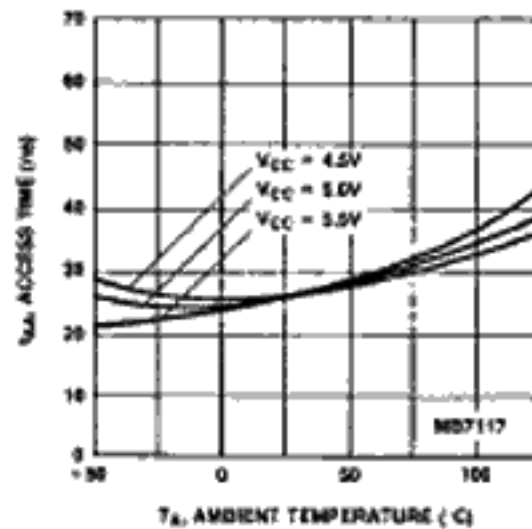
I_{OL} Output Low Current vs. V_{OL} Output Low Voltage



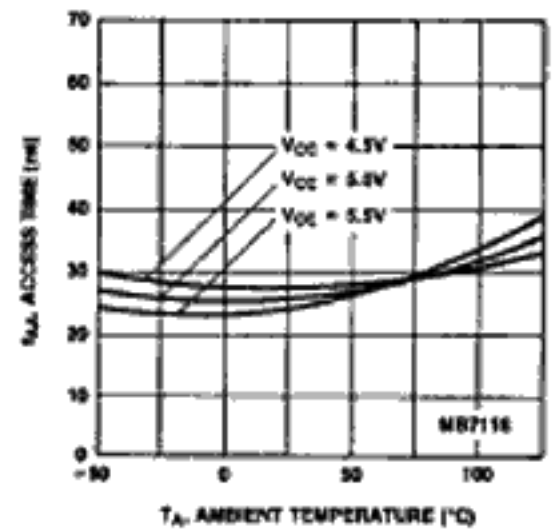
I_{OH} Output High Current vs. V_{OH} Output High Voltage



t_{AA} Access Time vs. Ambient Temperature



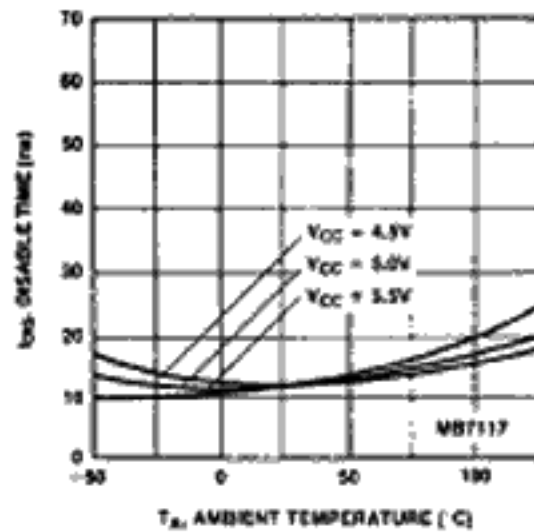
t_{AA} Access Time vs. Ambient Temperature



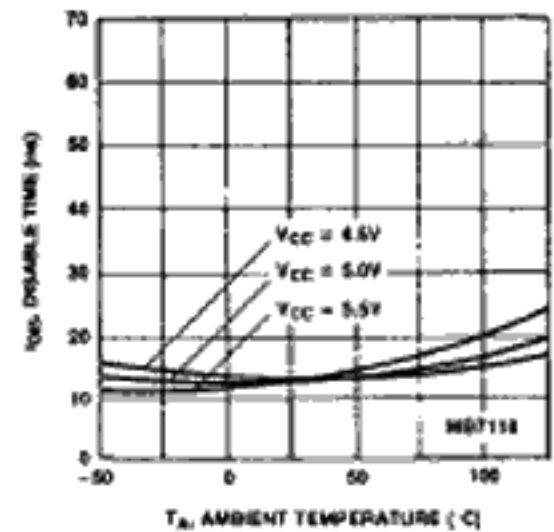
MB7117E/H
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Typical Characteristics
Curves
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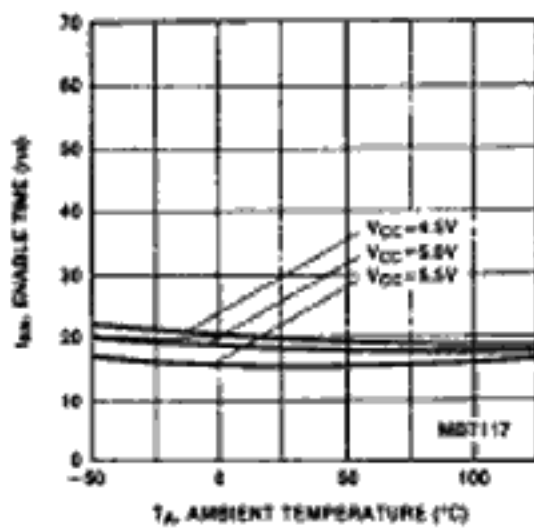
t_{OS} Disable Time
vs. Ambient Temperature



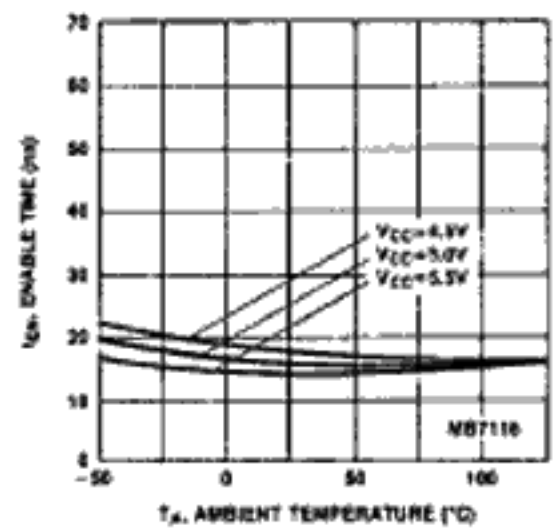
t_{OS} Disable Time
vs. Ambient Temperature



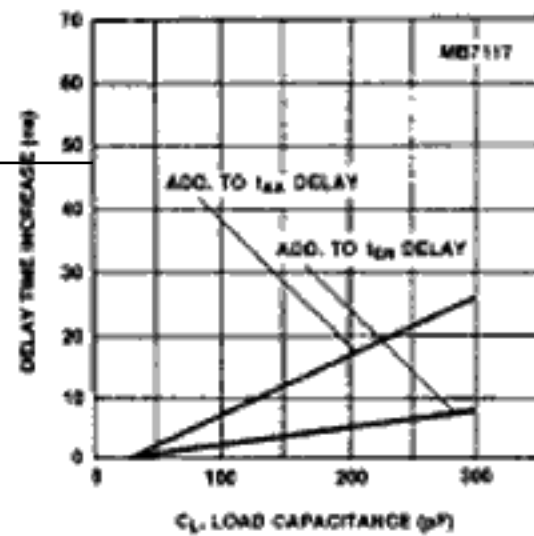
t_{EN} Enable Time
vs. Ambient Temperature



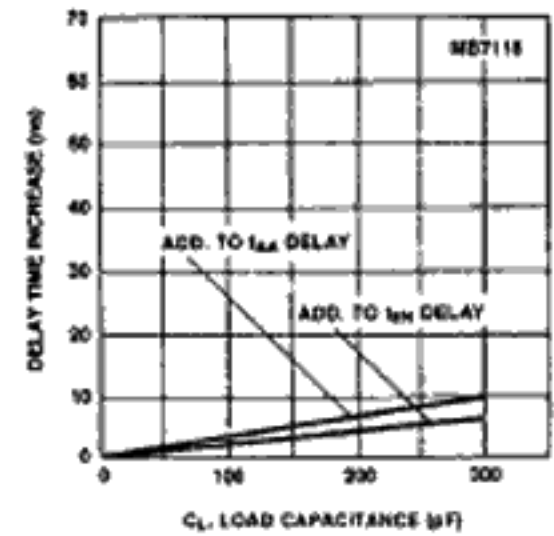
t_{EN} Enable Time
vs. Ambient Temperature



Delay Time Increase
vs. C_L Load Capacitance



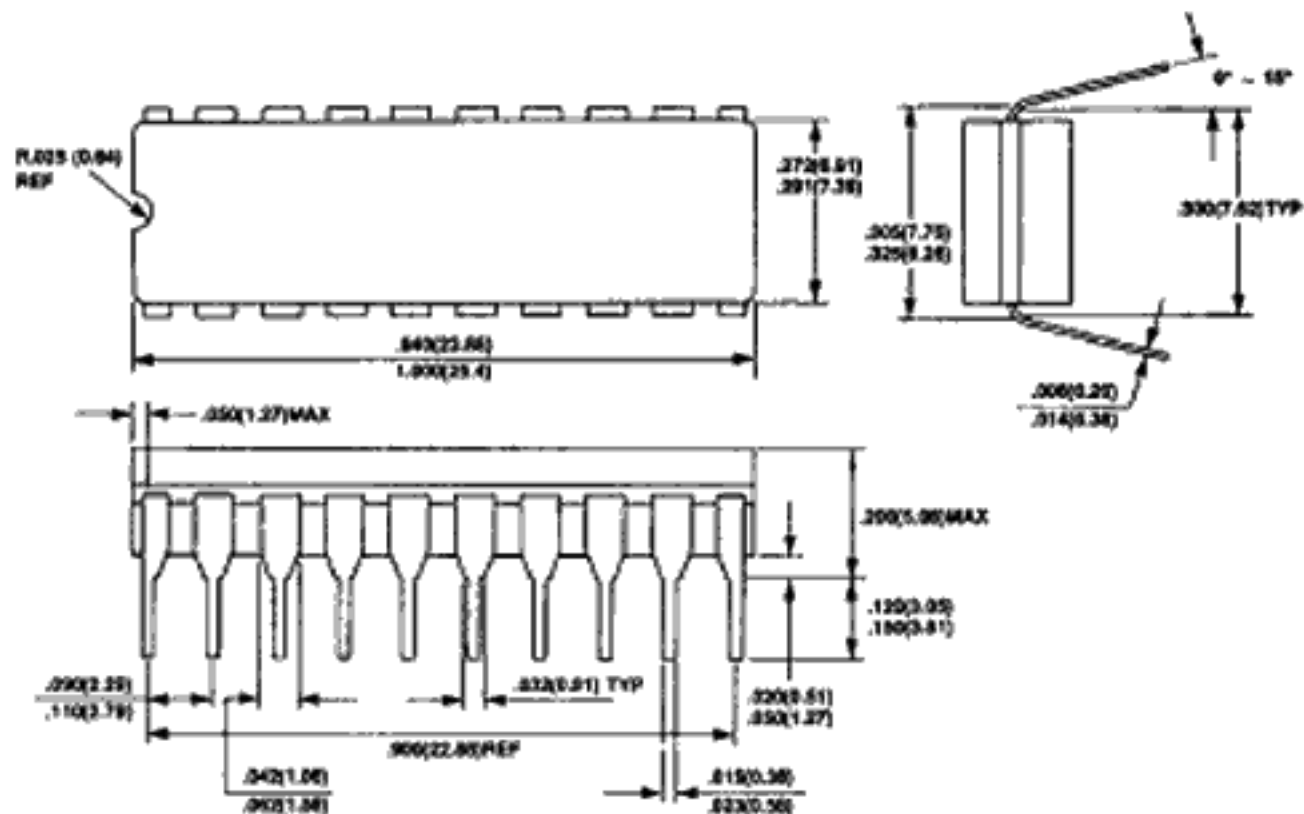
Delay Time Increase
vs. C_L Load Capacitance



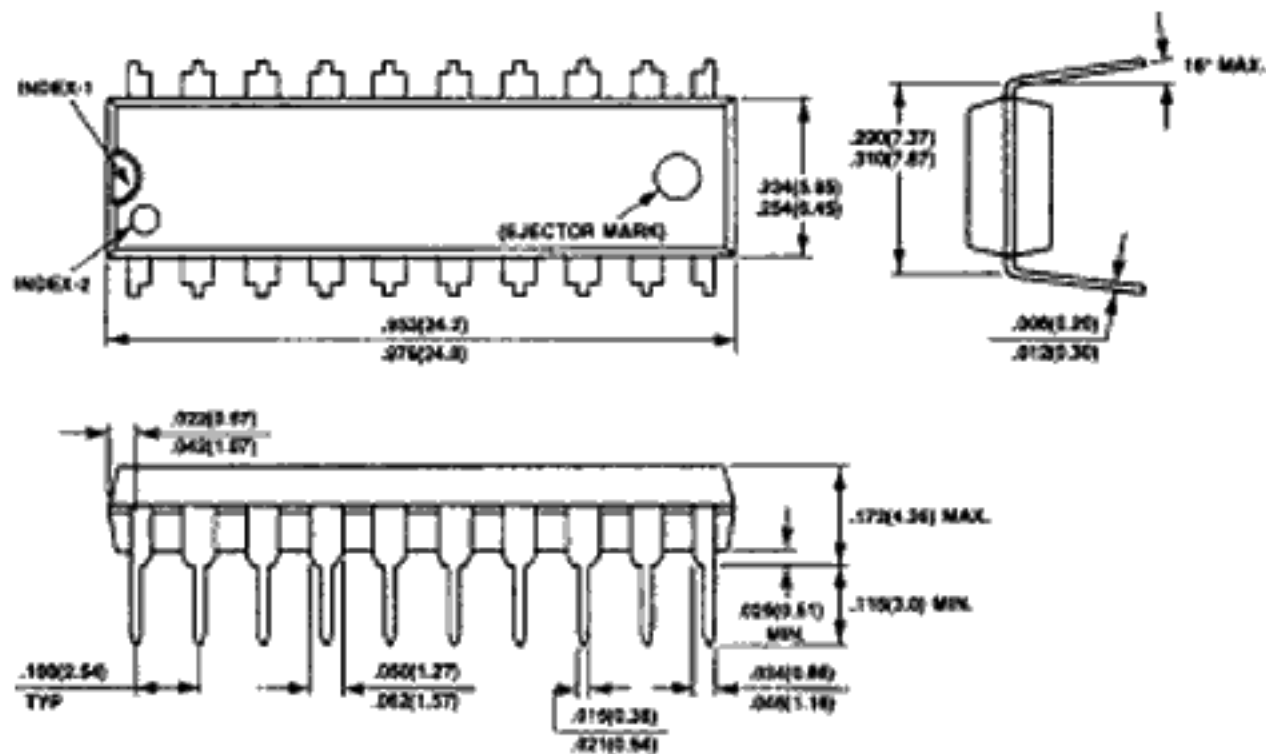
MB7117E/H
MB7118E/H

Package Dimensions
Dimensions in inches
(millimeters)

**20-Pin Cerdip Dual In-Line Package
DIP-20C-C01**



**20-Pin Plastic Dual In-Line Package
DIP-20P-M02**



MB7117E/M
MB7118E/M

Package Dimensions

(Continued)
Dimensions in inches
(millimeters)

**20-Pad Ceramic (Frit Seal) Leadless Chip Carrier
(Case No.: LCC-20C-F02)**

