April 1990
Edition 3.0

FUJITSU

DATA SHEET

MB7111E/H/7112E/H/Y/7111L/7112L

PROGRAMMABLE SCHOTTKY 256-BIT READ ONLY MEMORY

SCHOTTKY 256-BIT DEAP PROM (32 WORDS x 8 BITS)

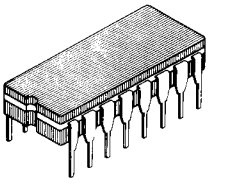
The Fujitsu MB7111 and MB7112 are high speed Schottky TTL electrically field programmable read only memories organized as 32 words by 8-bits. With uncommitted collector outputs provided on the MB7111 and three-state outputs on the MB7112 memory expansion is simple.

The memory is fabricated with all logic "zeros" (positive logic). Logic level "ones" can be programmed by the highly reliable DEAP (Diffused Eutectic Aluminum Process) according to simple programming procedures.

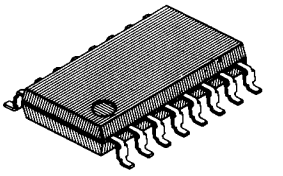
The sophisticated passive isolation termed SVG (Shallow V-Groove) with thin epitaxial layer and Schottky TTL process permits minimal chip size and fast access time.

The extra test cells and unique testing methods provide enhanced correlation between programmed and unprogrammed circuits in order to perform AC, DC and programming test prior to shipment. This results in extremely high programmability.

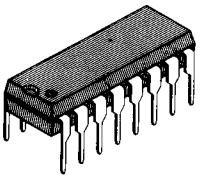
- Single +5V supply voltage.
- Low current PNP inputs.
- Power supply current:
  100 mA max. (E/H/Y)
  40 mA max. (L)
- Proven high programmability and reliability.
- Programming by DEAP (Diffused Eutectic Aluminum Process).
- Fast access time,
  Y: 15 ns typ, 20 ns max.
  H: 15 ns typ, 25 ns max.
  E: 15 ns typ, 35 ns max.
  L: 35 ns typ, 50 ns max.
- TTL compatible inputs and outputs.
- Open collector outputs (MB7111)
- 3-state outputs (MB7112)
- Two chip enable loads for simplified memory expansion.
- JEDEC approned pin out



CERAMIC PACKAGE
DIP-16C-C02



PLASTIC PACKAGE
FPT-16P-M02



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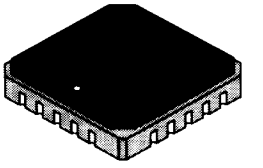

CERAMIC PACKAGE
LCC-20C-F02

ABSOLUTE MAXIMUM RATINGS (see NOTE)

Parameter		Symbol	Value	Unit
Power Supply Voltage		V_{CC}	−0.5 to +7.0	V
Power Supply Voltage (during programming)		V_{CCP}	−0.5 to +7.5	V
Input Voltage		V_{IN}	−1.5 to +5.5	V
Input Voltage (during programming)		V_{IPRG}	22.5	V
Output Voltage (during programming)		V_{OPRG}	−0.5 to +22.5	V
Input Current		I_{IN}	−20	mA
Input Current (during programming)		I_{IPRG}	+270	mA
Output Current		I_{OUT}	+100	mA
Output Current (during programming)		I_{OPRG}	+150	mA
Storage Temperature	Ceramic	T_{STG}	−65 to +150	°C
	Plastic		−40 to +125	
Output Voltage		V_{OUT}	−0.5 to V_{CC}	V

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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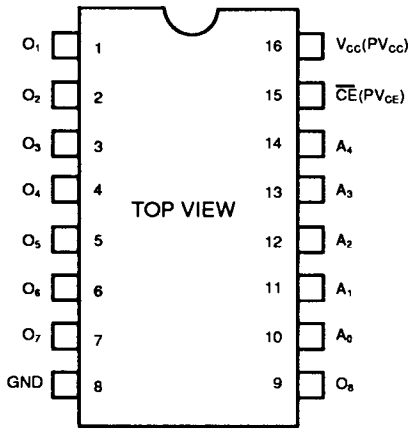
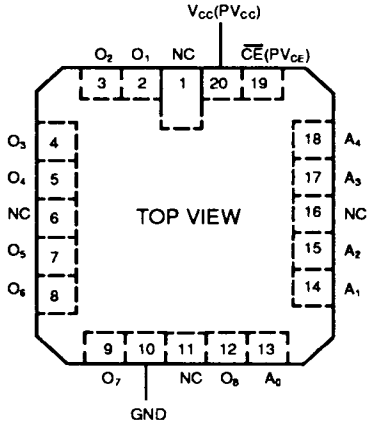
PIN ASSIGNMENT



PAD CONFIGURATION

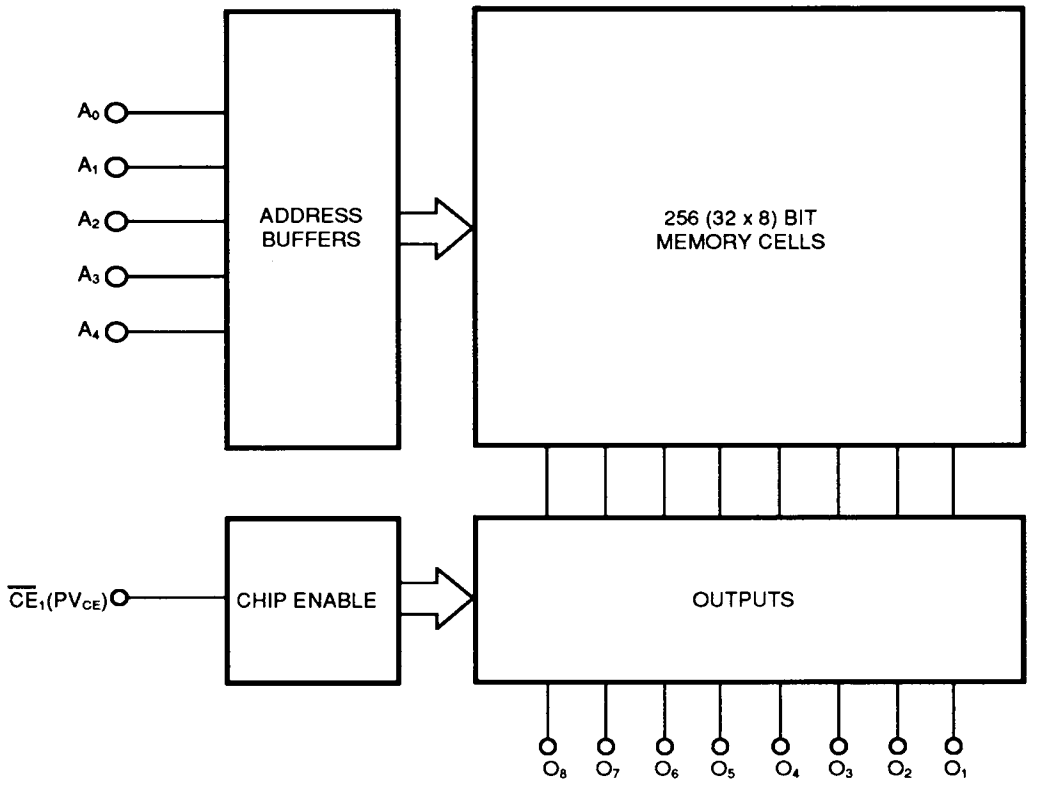


MODE SELECTION

Mode	$\overline{CE}$	Output 01 ~ 08
READ	V_{IL}	D_{OUT}
CHIP-DISABLE	V_{IH}	Hz
WRITE	PV_{CE}	Hz

D_{OUT} : Memory anser
Hz : High-impedance
PV_{CE} : 20 V (See programming information)

Fig.1 – MB7111/7112 BLOCK DIAGRAM



CAPACITANCE (f = 1MHz, V_{CC} = +5V, V_{IN} = +2V, T_A = 25°C)

Parameter	Symbol	Min	Typ	Max	Unit
Input Capacitance	C_I			10	pF
Output Capacitance	C_O			12	pF

GUARANTEED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
Input Low Voltage	V_{IL}	0		0.8	V
Input High Voltage	V_{IH}	2.0		5.5	V
Ambient Temperature	T_A	0		75	°C

DC CHARACTERISTICS

(Full guaranteed operating conditions unless otherwise noted)

Parameter		Symbol	Min	Typ	Max	Unit
Input Leakage Current (V_{IH} = 5.5V)		I_R			40	µA
Input Low Current (V_{IL} = 0.45V)		I_F			–250	µA
Output Low Voltage	I_{OL} = 10 mA	V_{OL}			0.45	V
	I_{OL} = 16 mA				0.50	
Output Leakage Current (V_O = 2.4V, chip disabled)	MB7111	I_{OLK}			40	µA
Output Leakage Current (V_O = 2.4V, chip disabled)	MB7112	I_{OIH}			40	µA
Output Leakage Current (V_O = 0.45V, chip disabled)	MB7112	I_{OIL}			–40	µA
Input Clamp Voltage (I_{IN} = –18 mA)		V_{IC}			–1.2	V
Power Supply Current (V_{IN} = OPEN or GND)	E/H/Y	I_{CC}		70	100	mA
	L			25	40	
Output High Voltage (I_O = –2.4 mA)	MB7112	V_{OH}*	2.4			V
Output Short Circuit Current (V_O = GND)	MB7112	I_{OS}*	–1.5		–60	mA

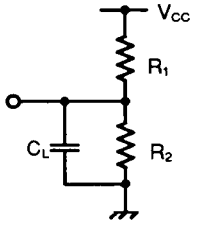
Notes: *1. Denote guaranteed characteristics of the output high-level (ON) state when the chip is enabled (V_{CE} ≤ 0.4V) and the programmed bit is addressed. These characteristics cannot be tested prior to programming, but are guaranteed by factor testing.

*2. This value denotes conditions at T_A = 25°C and V_{CC} = +5V.

Fig. 2 – AC TEST CONDITIONS

INPUT CONDITIONS
Amplitude..... 0V to 3V
Rise and Fall Time..... 5ns from 1V to 2V
Frequency..... 1MHz

LOAD CONDITION



	MB7111/MB7112		
	R_1	R_2	C_L
t_{AA}	300Ω	600Ω	30pF
t_{DIS}	300Ω	600Ω	30pF
t_{EN}	300Ω	600Ω	30pF

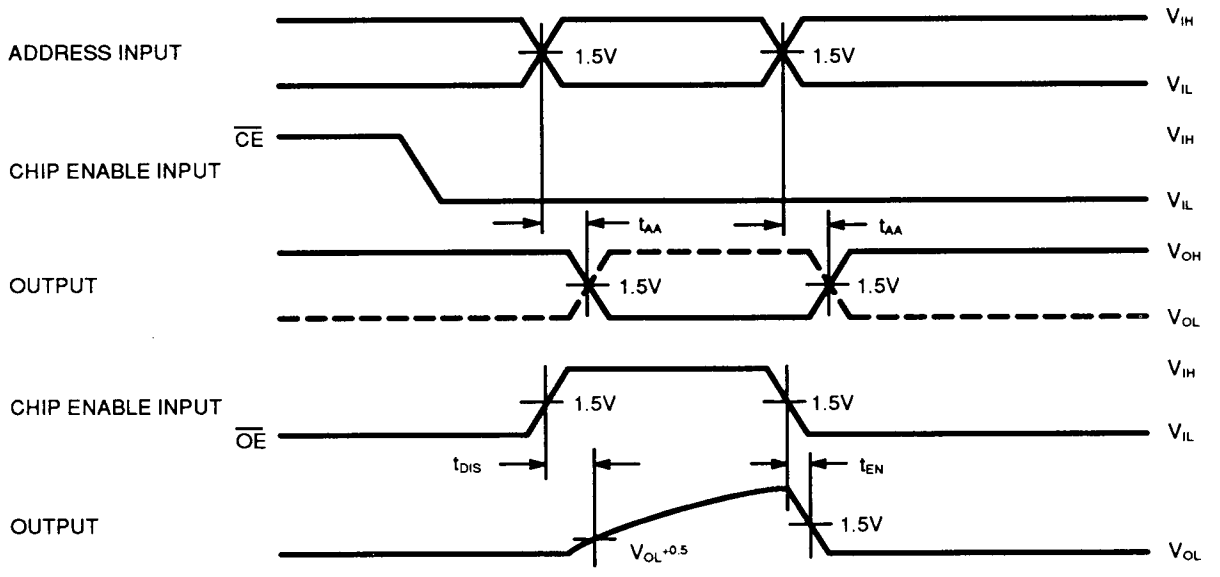
AC CHARACTERISTICS

(Full guaranteed operating conditions unless otherwise noted)

Parameter	Symbol	E		H		Y		L		Unit
		Typ	Max	Typ	Max	Typ	Max	Typ	Max	
Access Time (via address input)	t_{AA}	15	35	15	25	15	20	35	50	ns
Output Disable Time	t_{DIS}	15	25	15	20	15	20	20	30	ns
Output Enable Time	t_{EN}	10	20	10	20	10	15	20	30	ns

Note: Using Wired-OR outputs, this value is equivalent to the output enable time (t_{EN}) of the device.

OPERATION TIMING DIAGRAM



Note: Output disable time is the time taken for the output to reach a high impedance state when chip enable goes high. Output enable time is the time taken for the output to become active when chip enable goes low. The high impedance state is defined as a point on the output waveform, that is 0.5V from the active output level.

INPUT/OUTPUT CIRCUIT INFORMATION

INPUT

In the input circuit, Schottky TTL circuit technology is used to achieve high-speed operation. A PNP transistor in the first stage of input circuit remarkably improves input high/low current characteristics. Also, the input circuit includes a protection diode for reliable operation.

OPEN-COLLECTOR OUTPUT

Open-collector output is often utilized in high speed applications where power dissipation must be minimized. When the device is switched, there is no current sourced from the supply rail. Consequently, the current spike normally associated with TTL totempole outputs is eliminated. In high frequency applications, this minimizes noise problems (false triggering) as well as power drain. for example, the transient current (low impedance high-level to low impedance low-level) is typically 30mA for the MB7112 (3-state) compared to 0mA for the MB7111 (open-collector).

THREE-STATE OUTPUT

A "three-state" output is a logic element which has three distinct output states of ZERO, ONE and OFF (wherein OFF represents a high impedance condition which can neither sink nor source current at a definable logic level.) Effectively, then, the device has all the desirable features of a totem-pole TTL output (e.g., greater noise immunity, good rise time, line driving capacity), plus the ability to connect to bus-organized systems.

If two devices are on at the same time, the possibility exists that they may be in opposite low impedance states simultaneously, with short circuit current from one enabled device. While physical damage under these conditions is unlikely, system noise problems could result. Therefore, the system designer should ensure that this condition does not exist.

Fig. 3 – MB7111/7112 INPUT

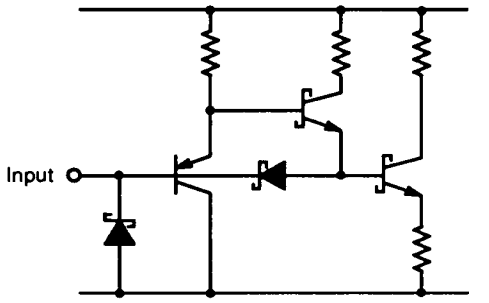


Fig. 4 – MB7111L/7112L INPUT

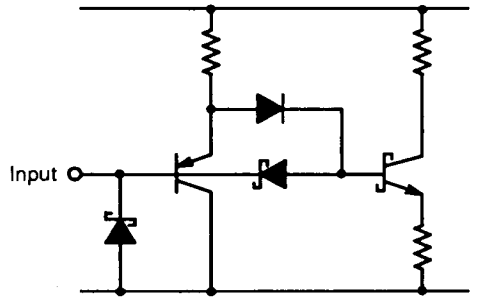
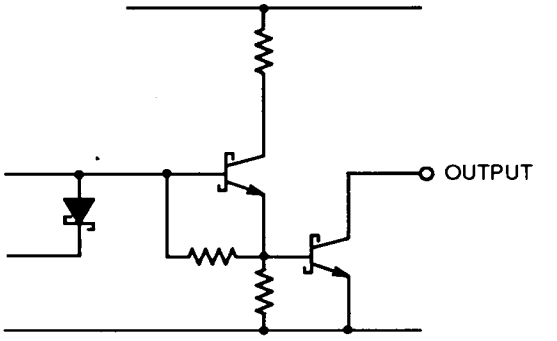


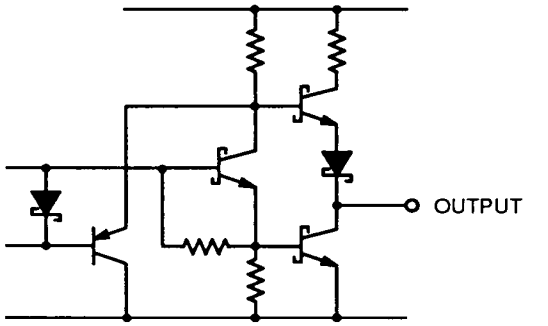
Fig. 5 – MB7111 OUTPUT



INPUT/OUTPUT CIRCUIT INFORMATION (Continued)

In the output circuit, Schottky TTL circuit technology is used to active high-speed operation. A PNP transistor in the output circuit decreases the load on the Chip Enable circuit.

Fig. 6 – MB7112 OUTPUT



TYPICAL CHARACTERISTICS CURVES

Fig. 7 – I_{INA} INPUT CURRENT vs. V_{IN} INPUT VOLTAGE

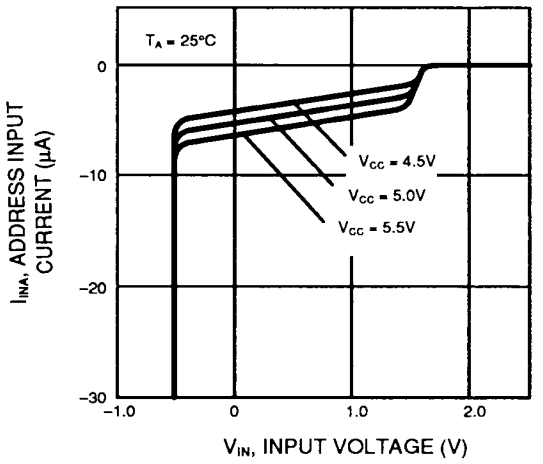
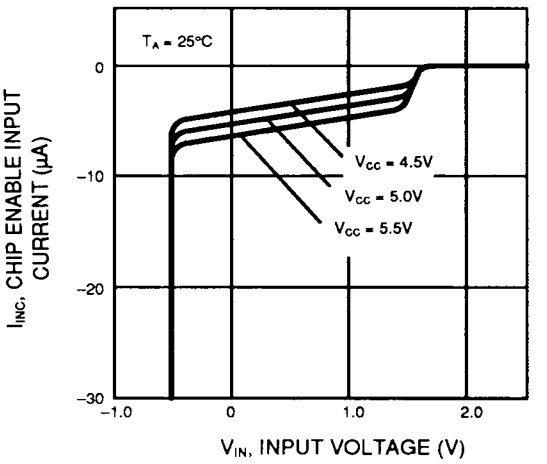


Fig. 8 – I_{INC} INPUT CURRENT vs. V_{IN} INPUT VOLTAGE



TYPICAL CHARACTERISTICS CURVES (Continued)

Fig. 9 – I_{OL} OUTPUT LOW CURRENT vs. V_{OL} OUTPUT LOW VOLTAGE

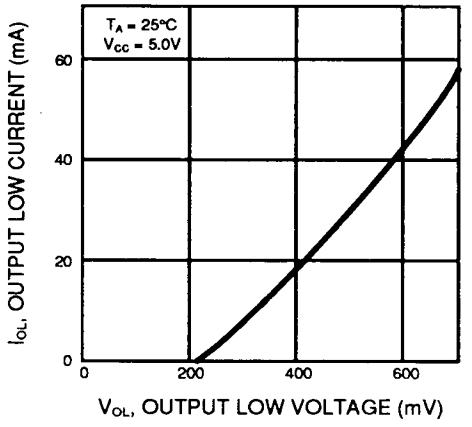


Fig. 10 – I_{OH} OUTPUT HIGH CURRENT vs. V_{OH} OUTPUT HIGH VOLTAGE

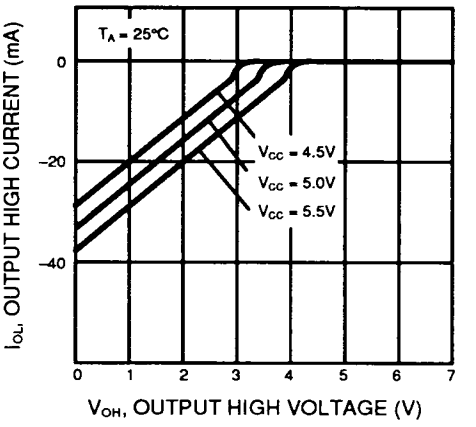


Fig. 11 – t_{AA} ACCESS TIME vs. AMBIENT TEMPERATURE

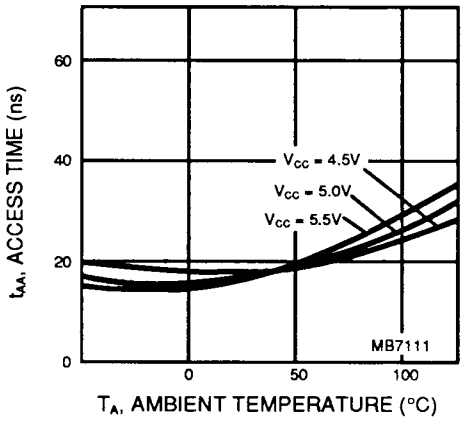


Fig. 12 – t_{AA} ACCESS TIME vs. AMBIENT TEMPERATURE

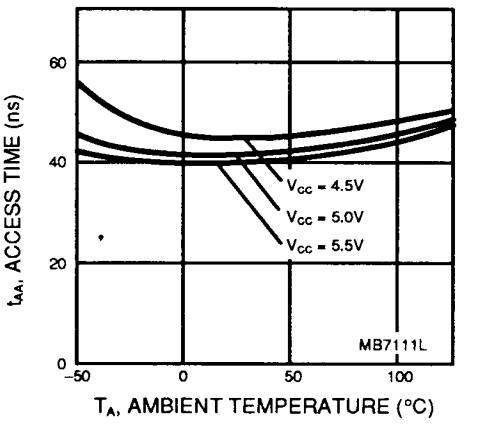


Fig. 13 – t_{AA} ACCESS TIME vs. AMBIENT TEMPERATURE

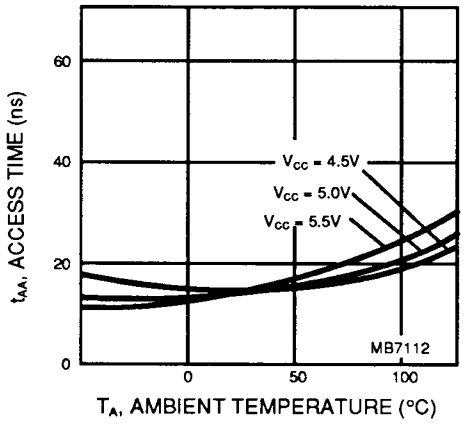
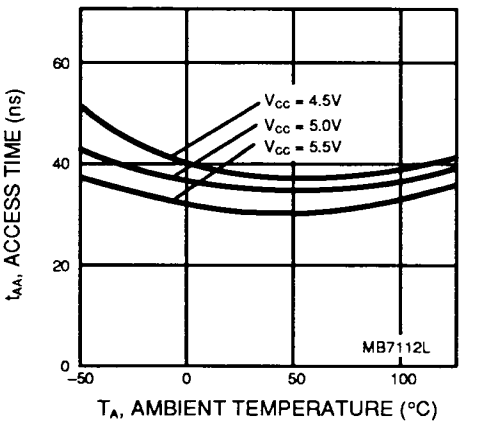


Fig. 14 – t_{AA} ACCESS TIME vs. AMBIENT TEMPERATURE



TYPICAL CHARACTERISTICS CURVES (Continued)

Fig. 15 – t_{DIS} DISABLE TIME vs. AMBIENT TEMPERATURE

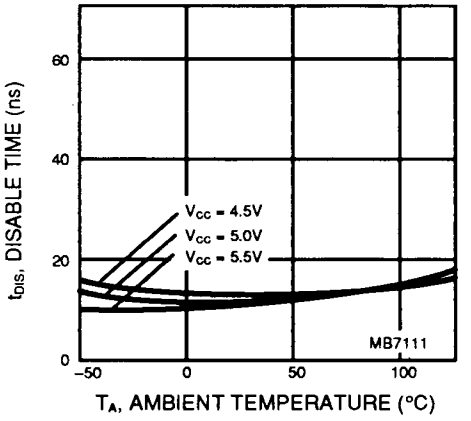


Fig. 16 – t_{DIS} DISABLE TIME vs. AMBIENT TEMPERATURE

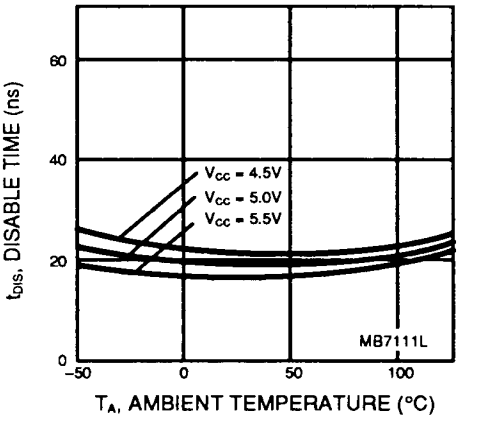


Fig. 17 – t_{DIS} DISABLE TIME vs. AMBIENT TEMPERATURE

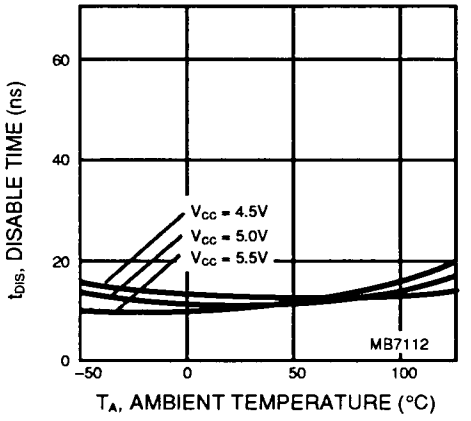


Fig. 18 – t_{DIS} DISABLE TIME vs. AMBIENT TEMPERATURE

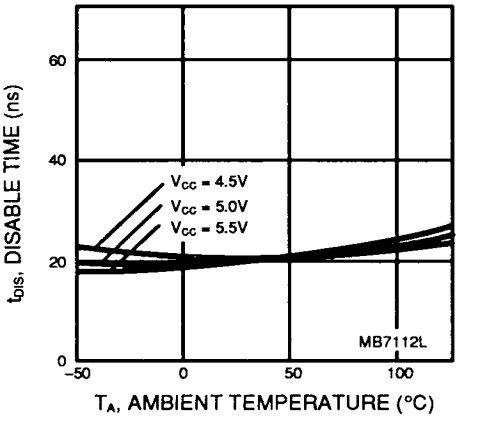


Fig. 19 – t_{EN} ENABLE TIME vs. AMBIENT TEMPERATURE

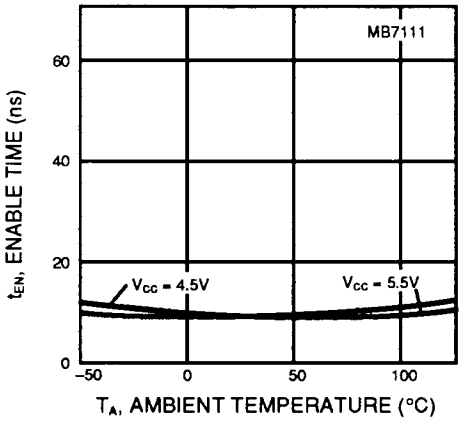
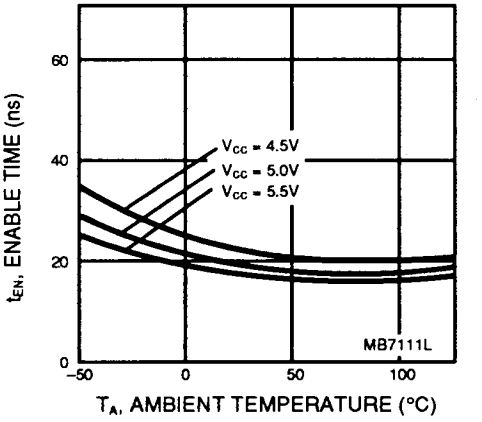


Fig. 20 – t_{EN} ENABLE TIME vs. AMBIENT TEMPERATURE



TYPICAL CHARACTERISTICS CURVES (Continued)

Fig. 21 – t_{EN} ENABLE TIME vs. AMBIENT TEMPERATURE

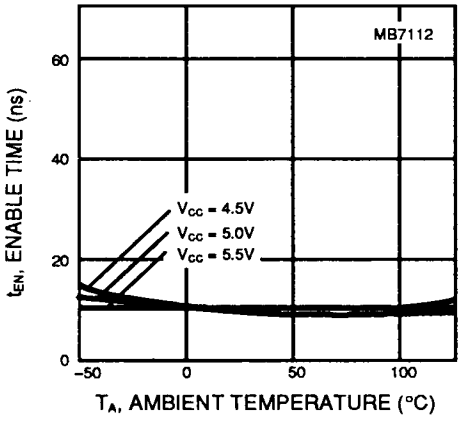


Fig. 22 – t_{EN} ENABLE TIME vs. AMBIENT TEMPERATURE

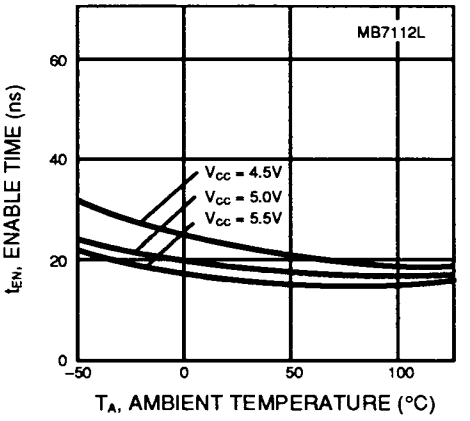


Fig. 23 – DELAY TIME INCREASE vs. C_L LOAD CAPACITANCE

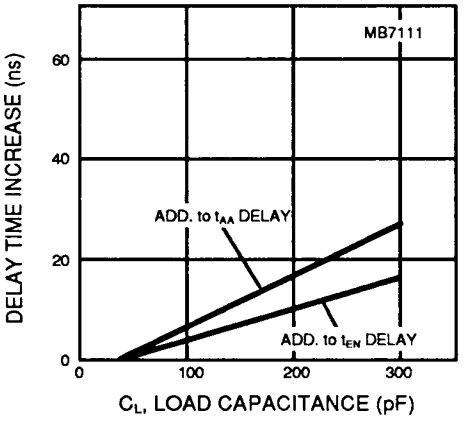


Fig. 24 – DELAY TIME INCREASE vs. C_L LOAD CAPACITANCE

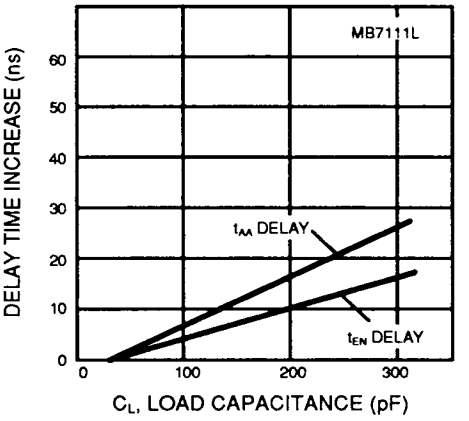


Fig. 25 – DELAY TIME INCREASE vs. C_L LOAD CAPACITANCE

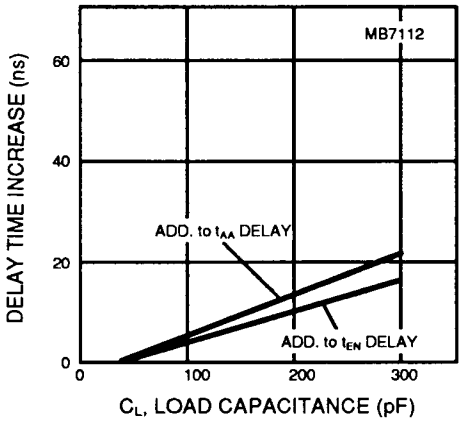
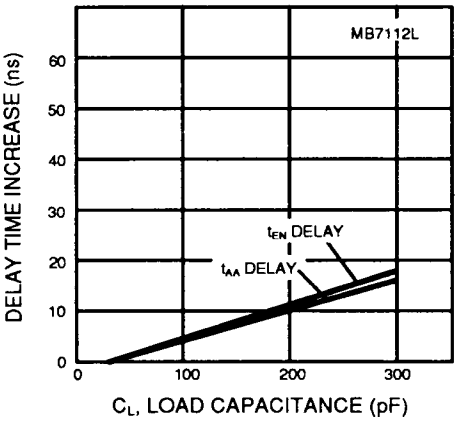


Fig. 26 – DELAY TIME INCREASE vs. C_L LOAD CAPACITANCE



PROGRAMMING INFORMATION

FUJITSU PROM TECHNOLOGY

The Fujitsu MB7100 series is the junction-shorting Schottky PROM. A memory cell consists of a programmable element of a PN diode and a vertically connected PNP transistor. The current blocking state of the reverse diode is changed to the current conducting state of the shorted-junction diode by programming. The programming element of the PN diode uses the N^+ and P^+ diffusion layer, the PNP transistor uses a P^+ diffusion layer, an N^+ epitaxial layer, and a P^- substrate (Fig. 27).

Each word line island is divided by passive isolations named IOP (Isolation by Oxide and Poly-silicon), and each memory cell in the same island is divided by the passive isolation named SVG (Shallow V-Grove). The vertical structure of the junction-shorting memory cell makes a high packing density possible.

In programming, reverse current pulses are applied to the cathod of the PN diode. This increases the temperature at the junction. When the temperature reaches the point where the silicon and aluminum form a eutectic, the eutectic diffuses from the surface of the the metal-silicon contact region to the anode of the PN diode, and results in junction shorting. This program technique was therefore named "Diffused Eutectic Aluminum Process" (DEAP).

Once the junction is shorted, the power dissipation at the junction decreases to less than one fifth, and the temperature decreases. This drop in temperature stops further diffusion of the eutectic, and protects the PNP transistor from destruction.

SPECIAL FACTORY TESTING

Extra rows and extra columns of test cells, plus additional circuitry built into the PROM chip, allow improved factory testing of DC, AC and programming characteristics. These test cells and test circuitry provide enhanced between

Fig. 27 – PROGRAMMED CELL (CROSS SECTION)

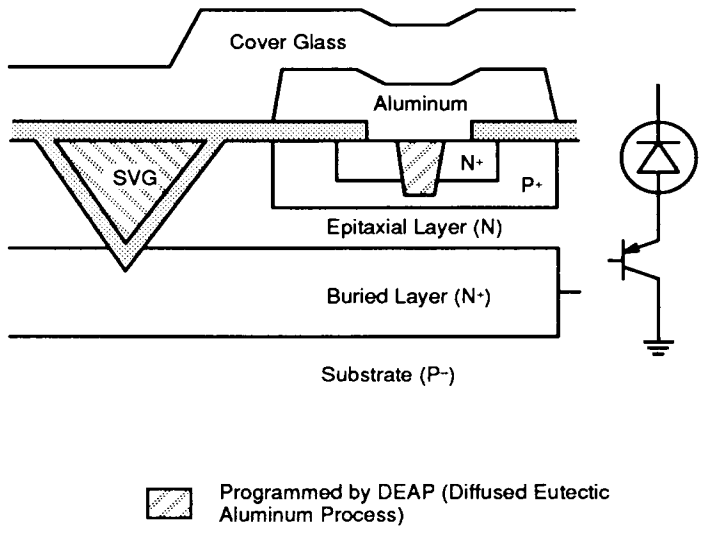
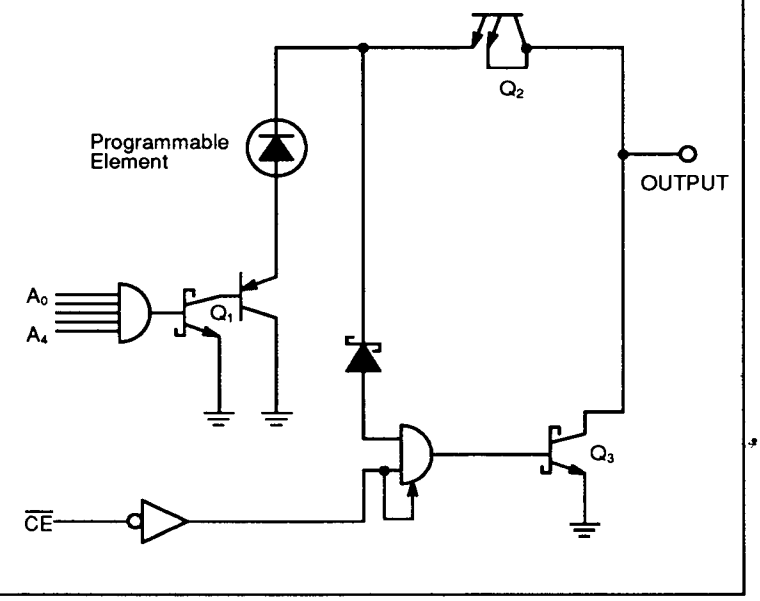


Fig. 28 – INTERNAL PROGRAMMING CIRCUIT



PROGRAMMING INFORMATION (Continued)

programmed and unprogrammed circuits in order to guarantee high programmability and reliability.

PROGRAMMING (in electrical view)

The device is manufactured with outputs low (positive logic "zero") in all storage cells. An output at the selected cell is charged to high (logic "one") by programming.

As shown in Fig. 28, transistor Q_1 is turned on to select the desired bit for programming by using five all address inputs. By applying the PV_{CE} pulse voltage, the chip is disabled and transistor Q_3 is held off. Then, a train of programming pulses applied to the desired output flows through transistor Q_2 and memory cell into transistor Q_1. This programming current changes the programmable element to the conducting state. The pulse train is stopped and two additional programming pulses are then applied to assure that the element is programmed properly, as soon as the output voltage indicates that the selected cell is in the logic "one" state. One output must be programmed at a time since the internal decoding circuit is capable of sinking only one unit of programming current at a time.

VERIFICATION

After the device has been programmed, the correct program pattern can be verified by taking chip enable input low. To guarantee full supply voltage and full temperature range operation, a programmed device should source 2.4mA at V_{OH} = 2.4V and V_{CC} = 7.0V at 25°C ambient temperature.

LIABILITY

Fujitsu utilizes an extensive testing procedure to ensure device performance prior to shipment. However, 100% programmability is not guaranteed, and it is imperative that this specification be rigorously adhered to in order to achieve a satisfactory programming yield. Fujitsu will not accept responsibility for any device found defective if it was not programmed according to this specification. Devices returned to Fujitsu as defective must be accompanied by a complete truth table with clearly indicated locations of supposedly defective memory cells.

DC SPECIFICATIONS (T_A = 25°C)

Parameter	Symbol		Min	Typ	Max	Unit
Input Low Level	V_{IL}		0		0.8	V
Input High Level	V_{IH}		2.0		5.25	V
Power Supply Voltage	PV_{CC}	P:	6.7	7.0	7.3	V
		R:	4.75	5.0	5.25	
Programming Pulse Current	I_{PRG}		120		130	mA
PV_{CE} Pulse Voltage	PV_{CE}		20	20	22	V
Programming Pulse Clamp Voltage	V_{PRG}		20	20	22	V
PV_{CE} Pulse Clamp Current	PI_{CE}		230		260	mA
Reference Voltage for a Prog. "1"	V_{REF}		1.0	1.5	2.4	V

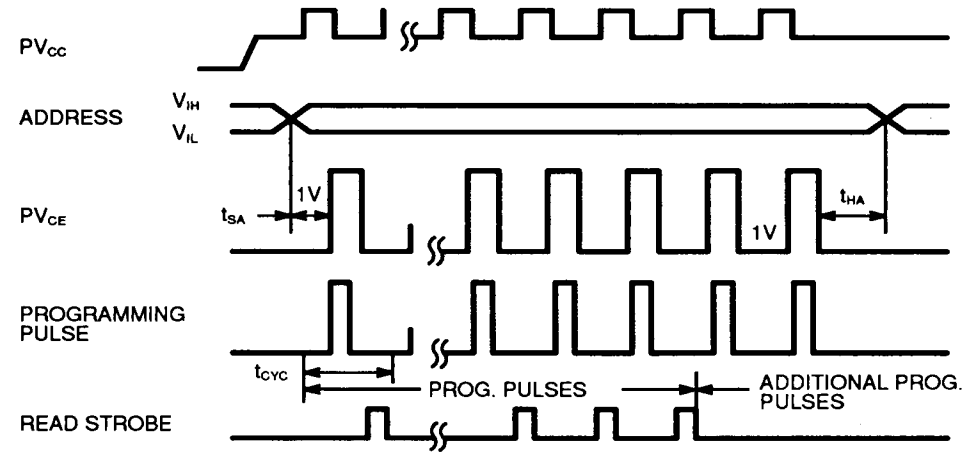
AC SPECIFICATIONS (T_A = 25°C)

Parameter	Symbol	Min	Typ	Max	Unit
Programming Pulse Cycle Time	t_{CYC}	40	50	60	µs
Programming Pulse Width	t_{PW}(1)	10	11	12	µs
Programming Pulse Rise Time	t_r(2)	–	–	2	µs
PV_{CE} Pulse Rise Time	t_r(3)	–	–	2	µs
PV_{CC} Pulse Rise Time	t_r(4)	–	–	2	µs
Programming Pulse Fall Time	t_f(5)	–	–	2	µs
PV_{CE} Pulse Fall Time	t_f(6)	–	–	2	µs
PV_{CC} Pulse Fall Time	t_f(7)	–	–	2	µs
Address Input Set-up Time	t_{SA}	2	–	–	µs
PV_{CE} Set-up Time	t_{SP}(8)	4	–	–	µs
PV_{CC} Pulse Set-up Time	t_{SV}	4	–	–	µs
Address Input Hold Time	t_{HA}	2	–	–	µs
PV_{CE} Hold Time	t_{HP}(9)	2	–	–	µs
PV_{CC} Pulse Hold Time	t_{HV}	2	–	–	µs
PV_{CE} Pulse Trailing Edge to Read Strobe Time	t_{PR}(10)	10	–	–	µs
Progframming Pulse Number	n	–	–	100	Times
Programming Time/Bit	–	120	150	6120	µs/bit
Additional Programming Pulse Number	–	2	2	2	Times

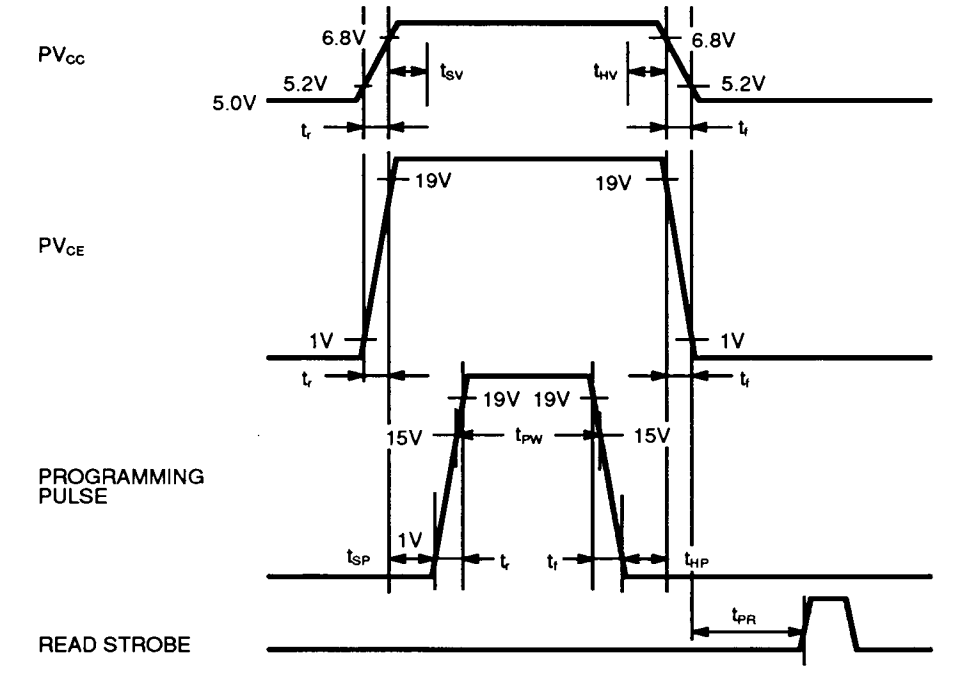
Note: (1) Stipulated 200Ω load and 15V.
(2) From 1V to 19V (200Ω load).
(3) From 1V to 19V.
(4) From 5.2V to 6.8V.
(5) From 19V to 1V (200Ω load).
(6) From 19V to 1V.
(7) From 6.8V to 5.2V.
(8) From PV_{CE} pulse 19V to programming pulse 1V.
(9) From programming pulse 1V to PV_{CE} pulse 19V.
(10) From PV_{CE} pulse 1V to read strobe.

PROGRAMMING INFORMATION (Continued)

TYPICAL WAVEFORMS



ONE DETAILED PROGRAMMING CYCLE



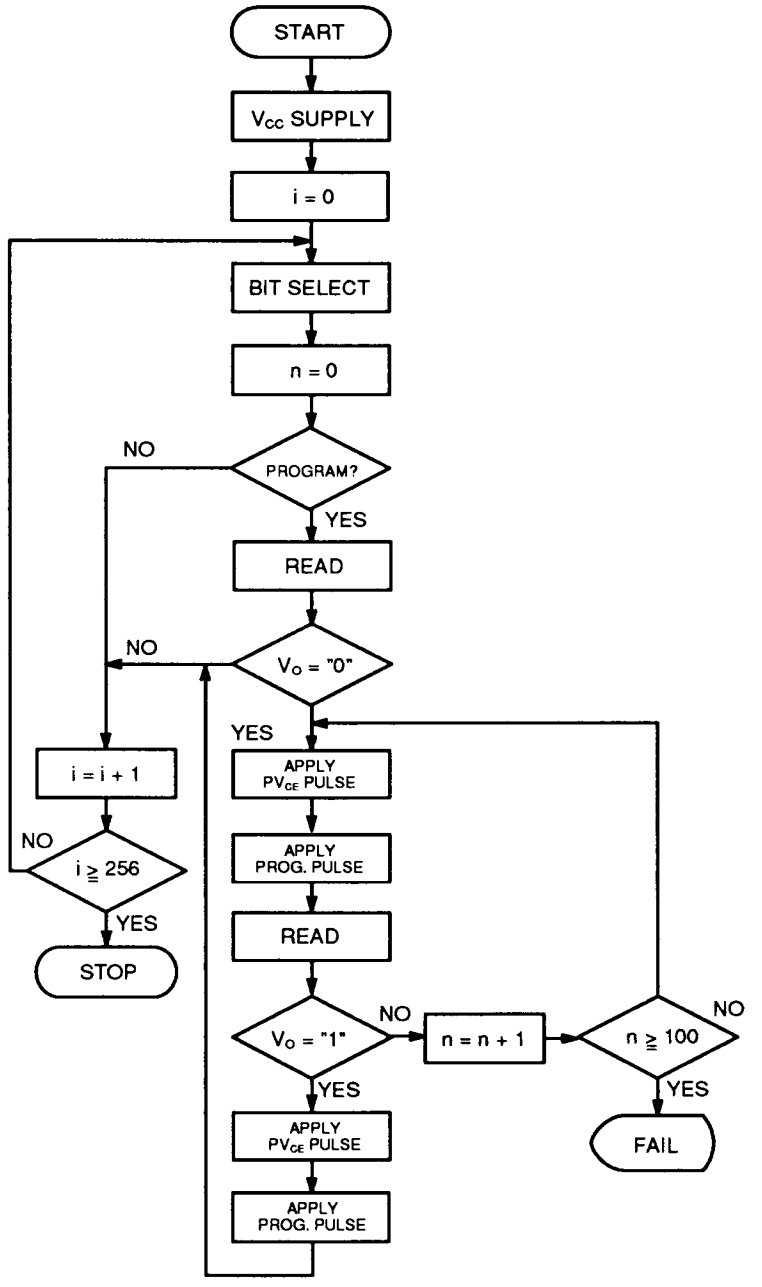
PROGRAMMING PROCEDURE

1. Apply power; $V_{CC} = PV_{CC}$, GND = 0V.
2. Select the desired bit.
3. Read the output to confirm the voltage V_O = low. (If V_O = high, select the next desired bit.)
4. Apply a 20V pulse voltage to the PV_{CE} input.
5. Apply a programming pulse with amplitude of 125 mA and duration of t_{PW} (11 µs) after a delay of t_{SP} (4 µs).
6. Read the output V_O after a delay of t_{PR} (10 µs).
   a) If V_O = low, repeat steps "4", "5" and "6" with cycle time of t_{CYC} (50 µs).
   b) If V_O = high, apply 2 additional programming pulses to provide a highly reliable memory cell.
7. Select the next desired bit after a delay of t_{HA} (2 µs).

NOTE:

1) Programming must be done bit by bit.
2) Ambient temperature during programming must be room temperature. (25°C ± 2°C)

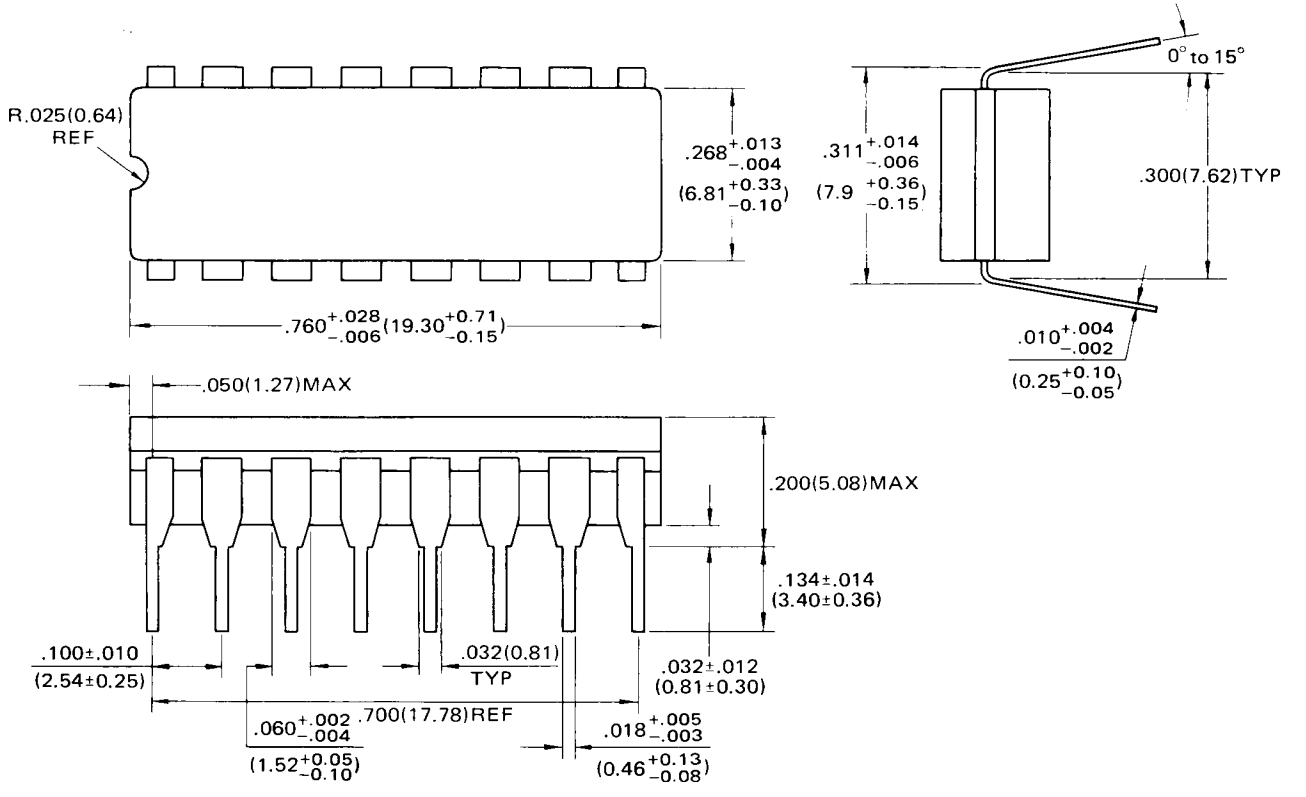
Fig. 29 – PROGRAMMING FLOW CHART



PACKAGE DIMENSIONS

Suffix (: -Z)

16-LEAD CERAMIC (CERDIP) DUAL IN-LINE PACKAGE
(CASE No.: DIP-16C-C02)

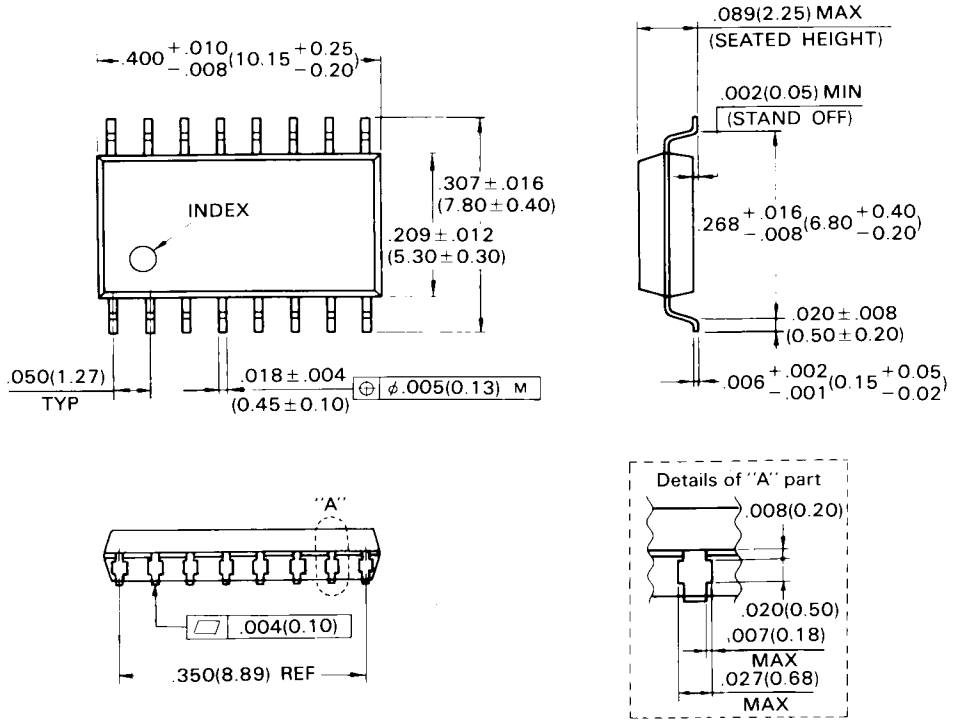


Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS (Continued)

Suffix (: -M)

16-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-16P-M02)

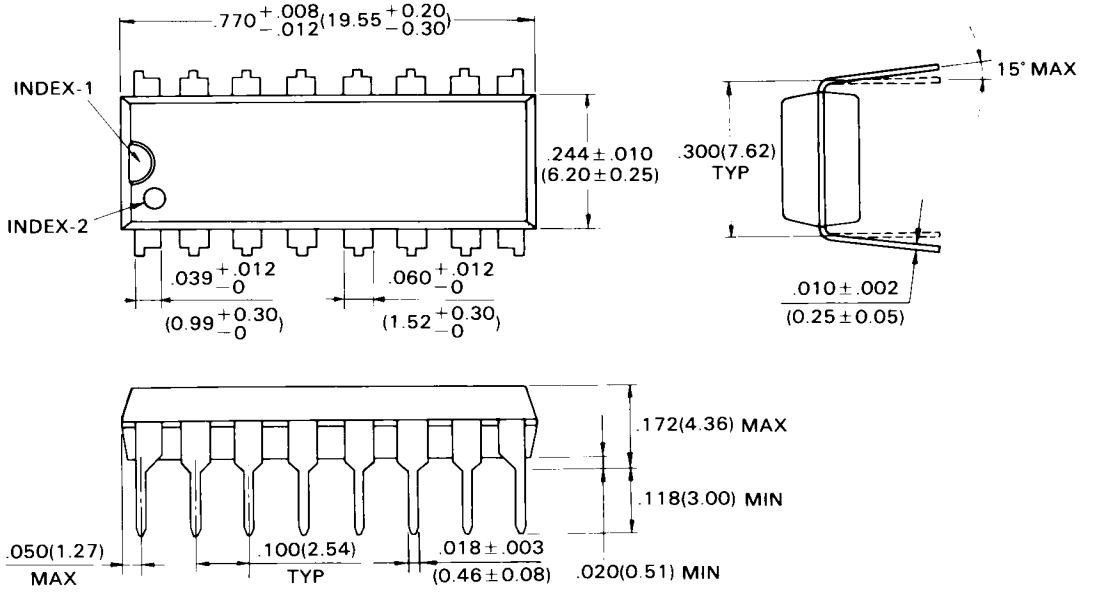


Dimensions in inches (millimeters)

PACKAGE DIMENSIONS (Continued)

Suffix (: -PF)

16-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-16P-M04)

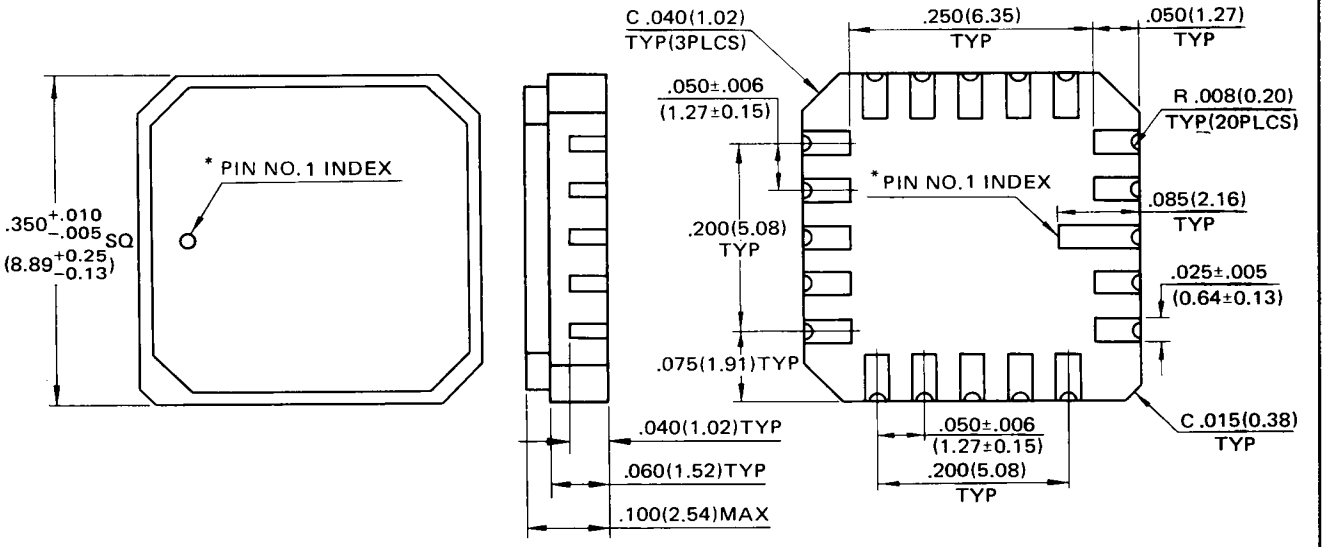


Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS (Continued)

(Suffix (: -TV)

20-PAD CERAMIC (FRIT SELL) LEADLESS CHIP CARRIER
(CASE No.: LCC-20C-F02)



* Shape of PIN NO. 1 INDEX: Subject to change without notice.

Dimensions in
inches (millimeters)