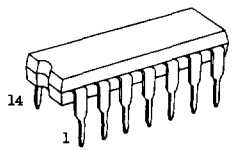
TC5029BP

C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TC5029BP QUAD 2-INPUT NAND GATE WITH N-CHANNEL OPEN DRAIN OUTPUT

TC5029BP contains four circuits of 2 input NAND gates having its respective outputs of N-channel open drain structure.

Since the drain voltage of output transistors are guaranteed up to 26 volts, these can be used for wide range of applications such as level shifters and drivers, and the wired OR arrangement is also easily obtained. Please utilize these for level shifters for P-channel MOS, controlling analog switches of positive/negative power supplies, etc.

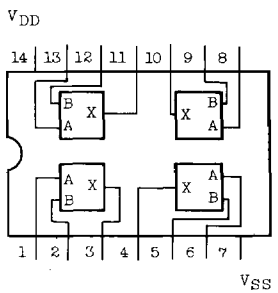


P(DIP14-P-300)

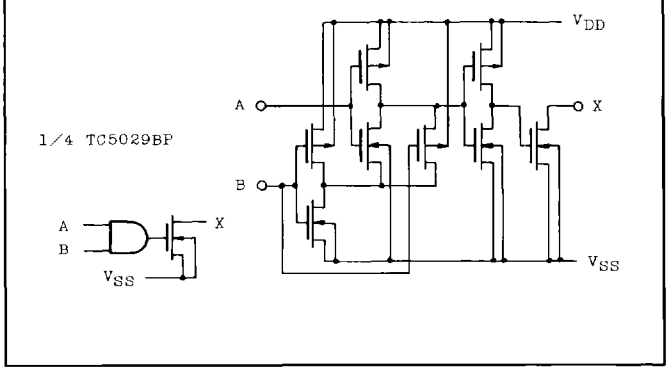
ABSOLUTE MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V_{DD}	V_{SS}-0.5 ~ V_{SS}+20	V
Input Voltage	V_{IN}	V_{SS}-0.5 ~ V_{DD}+0.5	V
Output Voltage	V_{OUT}	V_{SS}-0.5 ~ V_{SS}+26	V
DC Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300	mW
Storage Temperature Range	T_{stg}	-65 ~ 150	°C
Lead Temp./Time	T_{sol}	260°C · 10sec	

PIN ASSIGNMENT



CIRCUIT DIAGRAM



TRUTH TABLE

INPUTS		OUTPUT
B	A	X
L	L	HZ
L	H	HZ
H	L	HZ
H	H	L

HZ ; HIGH IMPEDANCE

RECOMMENDED OPERATION CONDITIONS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL		MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{DD}		3	-	18	V
Input Voltage	V_{IN}		0	-	V_{DD}	V
Output Voltage	V_{OUT}		0	-	24	V
Operating Temperature	T_{opr}		-40	-	85	°C

ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNIT
Low Level Output Voltage	V_{OL}	I_{OUT} <1μA $V_{IN}=V_{SS},V_{DD}$	5 10 15	- - -	0.05 0.05 0.05	- - -	0.00 0.00 0.00	0.05 0.05 0.05	- - -	0.05 0.05 0.05	V
Low Level Output Current	I_{OL}	V_{OL}=0.4V V_{OL}=0.5V V_{OL}=1.5V $V_{IN}=V_{SS},V_{DD}$	5 10 15	3.2 5.0 24.0	- - -	3.2 5.0 24.0		- - -	2.5 3.6 18.0	- - -	mA
High Level Input Voltage **	V_{IH}	V_{OUT}=0.5V,4.5V V_{OUT}=1.0V,9.0V V_{OUT}=1.5V,13.5V I_{OUT} <1μA	5 10 15	3.5 7.0 11.0	- - -	3.5 7.0 11.0	2.75 5.5 8.25	- - -	3.5 7.0 11.0	- - -	V
Low Level Input Voltage **	V_{IL}	V_{OUT}=0.5V,4.5V V_{OUT}=1.0V,9.0V V_{OUT}=1.5V,13.5V I_{OUT} <1μA	5 10 15	- - -	1.5 3.0 4.0	- - -	2.25 4.5 6.75	1.5 3.0 4.0	- - -	1.5 3.0 4.0	
Output off Leakage Current	I_{DH}	V_{OH}=24V	-	-	0.5	-	10^{-3}	0.5	-	50	μA
Input Current High Level	I_{IH}	V_{IH}=18V	18	-	0.3	-	10^{-5}	0.3	-	1.0	μA
Input Current Low Level	I_{IL}	V_{IL}=0V	18	-	-0.3	-	-10^{-5}	-0.3	-	-1.0	
Quiescent Current Consumption	I_{DD}	$V_{IN}=V_{SS},V_{DD}$ *	5 10 15	- - -	1.0 2.0 4.0	- - -	0.001 0.001 0.002	1.0 2.0 4.0	- - -	7.5 15 30	μA

* All valid input combinations. Outputs open.
** R_L=20KΩ

SWITCHING CHARACTERISTICS (Ta=25°C, V_{SS}=OV)

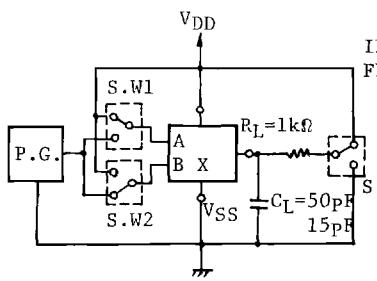
CHARACTERISTIC	SYMBOL	TEST CONDITIONS	V_{DD} (V)	MIN.	TYP.	MAX.	UNIT
Output Fall Time	t_{THL}	C_L=50pF	5	-	85	200	ns
			10	-	30	80	
			15	-	20	60	
(Low-High) Propagation Delay Time	t_{pLH}	R_L=1KΩ, C_L=15pF	5	-	230	500	ns
			10	-	120	200	
			15	-	100	150	
(High-Low) Propagation Delay Time	t_{pHL}	R_L=1KΩ, C_L=15pF	5	-	260	500	
			10	-	90	200	
			15	-	60	150	
(Low-High) Propagation Delay Time	t_{pLH}	R_L=10KΩ, C_L=15pF	5	-	830	1200	ns
			10	-	680	1000	
			15	-	610	850	
(High-Low) Propagation Delay Time	t_{pHL}	R_L=10KΩ, C_L=50pF	5	-	270	500	
			10	-	95	200	
			15	-	63	150	
Input Capacitance	C_{IN}			-	5	7.5	pF
Output Off Capacitance	C_{OUT}			-	25	-	pF

SWITCHING TIME TEST CIRCUIT AND WAVEFORM

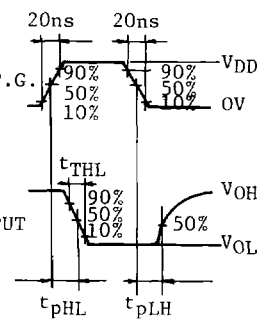
TEST CONDITION

No.	S.W1	S.W2	S.W3
1	P.G	V_{DD}	V_{DD}
2	V_{DD}	P.G	V_{DD}
3	P.G	P.G	V_{DD}

TEST CIRCUIT



WAVEFORM



(f_{IN}=50kHz, DUTY RATIO=50%)