TC40H373P/F

C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TC40H373 OCTAL D-TYPE LATCH (3-STATE OUTPUT)

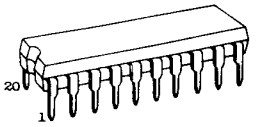
The TC40H373 is an octal D-type latch having 3-stage output control terminal.

When OUTPUT-CONTROL input is at "L" level, if ENABLE is set to "H" level, data is outputted as it is, and if ENABLE input to "L" level, data immediately before ENABLE input goes from "H" level to "L" level is held.

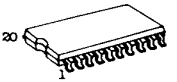
Further, when OUTPUT-CONTROL input is set to "H" level, high impedance is given to output regardless of the other inputs.

Eight circuits are common to OUTPUT-CONTROL input and ENABLE input.

The function and pin assignmnet of this latch are the same as those of the 74LS373.



DIP20(3D20A-P)

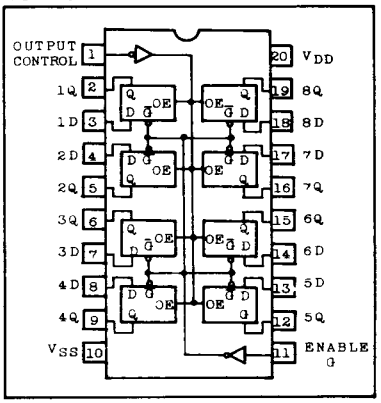


MFP20(F2 0A-P)

MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	V_{SS}-0.5 ∿ V_{SS}+10	V
Input Voltage	V_{IN}	V_{SS}-0.5 ∿ V_{DD}+0.5	V
Output Voltage	V_{OUT}	V_{SS}-0.5 ∿ V_{DD}+0.5	V
Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300(DIP)/180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temp./Time	T_{sol}	260°C · 10 sec	

PIN CONNECTION

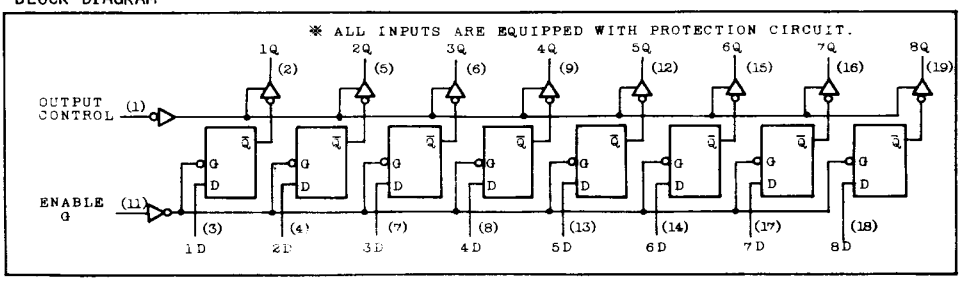


TRUTH TABLE

INPUTS			OUTPUT
OUTPUT CONTROL	ENABLE G	DATA	Q
L	H	H	H
L	H	L	L
L	L	※	Qo
H	※	※	High Impedance

※= Don't care

BLOCK DIAGRAM



RECOMMENDED OPERATING CONDITIONS (V_{SS}=0.0V)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{DD}	-	2.0	-	8.0	V
Input Voltage	V_{IN}	-	0	-	V_{DD}	V
Operating Temperature	T_{opr}	-	-40	-	85	°C

ELECTRICAL CHARACTERISTIC (V_{SS}=0.0V)

CHARACTERISTIC		SYMBOL	TEST CONDITION	V_{DD} (V)	40°C		25°C			85°C		UNIT
					MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
High Level Output Voltage		V_{OH}	$\|I_{OUT}\|$<1μA V_{IN}=V_{SS},V_{DD}	5	4.95	-	4.95	5.0	-	4.95	-	V
Low Level Output Voltage		V_{OL}	$\|I_{OUT}\|$<1μA V_{IN}=V_{DD},V_{SS}	5	-	0.05	-	0.0	0.05	-	0.05	V
High Level Output Current		I_{OH}	V_{OH}=4.6V V_{IN}=V_{SS},V_{DD}	5	-0.95	-	-0.88	-	-	-0.8	-	mA
Low Level Output Current		I_{OL}	V_{OL}=0.4V V_{IN}=V_{DD},V_{SS}	5	4.7	-	4.4	-	-	4.0	-	mA
Input Voltage	"H" Level	V_{IH}	$\|I_{OUT}\|$<1μA V_{OUT}=0.5V	5	4.0	-	4.0	-		-		V
	"L" Level	V_{IL}	V_{OUT}=4.5V	5	-	1.0	-	-	1.0	-	1.0	V
Input Current	"H" Level	I_{IH}	V_{IH}=8.0V	8	-	0.3	-	10^{-5}	0.3	-	1.0	μA
	"L" Level	I_{IL}	V_{IL}=0.0V	8	-	-0.3	-	-10^{-5}	-0.3	-	-1.0	μA
Output Disable Current	"H" Level	I_{DH}	V_{DH}=8.0V	8	-	0.5	-	10^{-4}	0.5	-	5	μA
	"L" Level	I_{DL}	V_{DL}=0.0V	8	-	-0.5	-	-10^{-4}	-0.5	-	-5	μA
Quiescent Supply Current		I_{DD}	*V_{IN}=V_{SS},V_{DD}	5	-	12.5	-	10^{-3}	12.5	-	75	μA

* All valid input combinations.

SWITCHING CHARACTERISTIC(Ta=25°C, V_{SS}=0V, V_{DD}=5V, C_L=50pF, R_L=1kΩ)

CHARACTERISTIC		SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Rise Time		t_{or}	Fig.1	-	15	30	ns
Output Fall Time		t_{of}		-	13	30	ns
Propagation Time	Low-High	t_{pLH}	DATA - Q Fig.1	-	38	57	ns
	High-Low	t_{pHL}		-	32	48	ns
Propagation Time	Low-High	t_{pLH}	ENABLE - Q Fig.1	-	39	59	ns
	High-Low	t_{pHL}		-	35	53	ns
Output Disable Time	High Level	t_{pHZ}	OUTPUT CONTROL - Q Fig.2, 3	-	25	40	ns
	Low Level	t_{pLZ}		-	27	40	ns
Output Enable Time	High Level	t_{pZH}		-	27	40	ns
	Low Level	t_{pZL}		-	30	45	ns
Minimum Enable Pulse Width		t_w	Fig.1	-	9	20	ns
Minimum Set up Time		t_{set-up}	Fig.1	-	5	10	ns
Minimum Hold Time		t_{hold}		-	0	-	ns
Input Capacitance		C_{IN}		-	5	-	pF
Output Capacitance		C_{OUT}		-	12	-	pF

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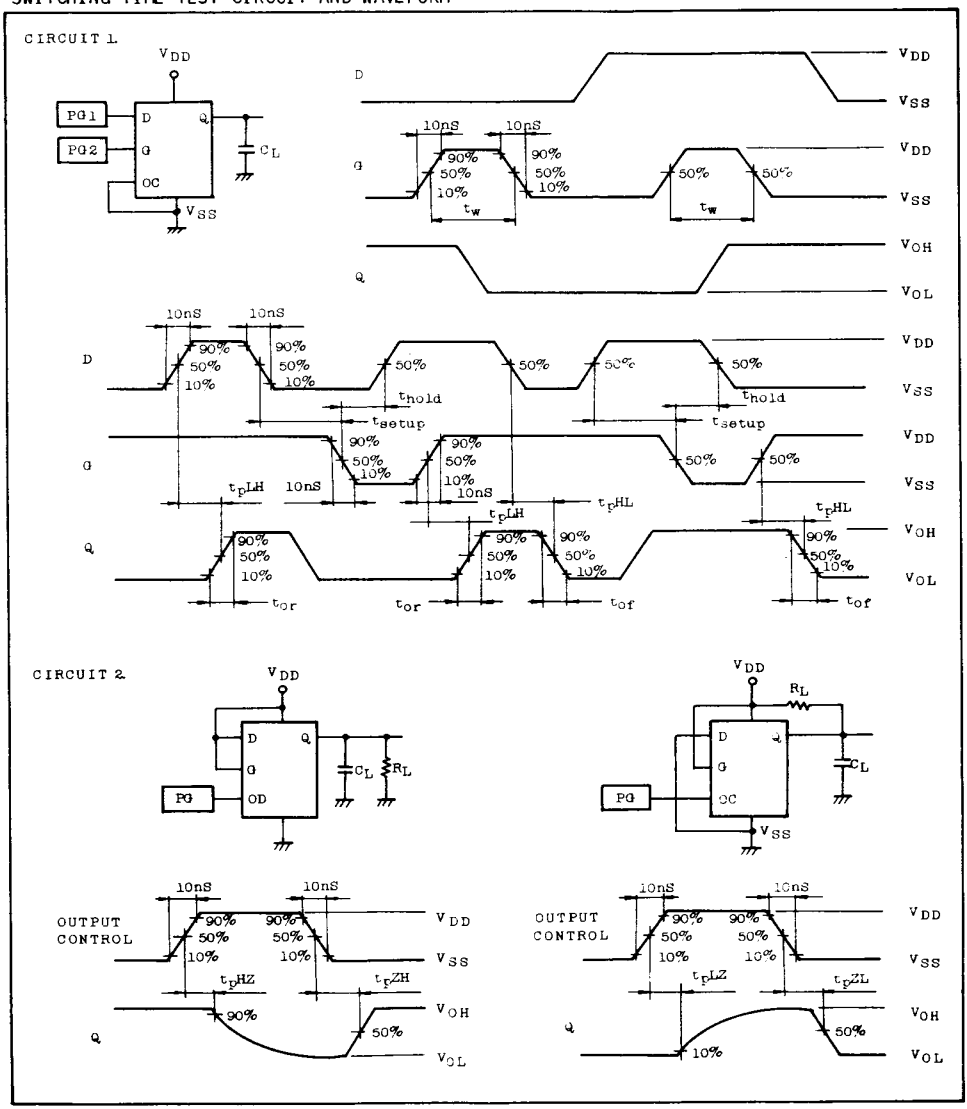
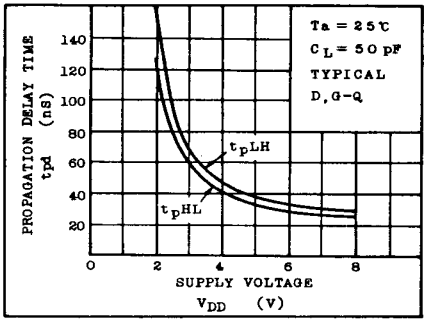
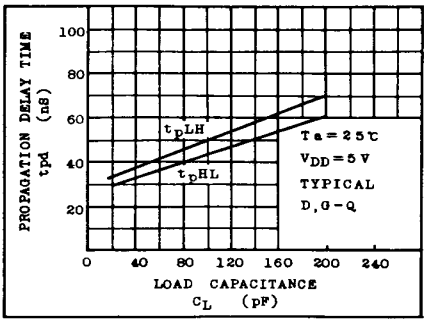
SWITCHING TIME TEST CIRCUIT AND WAVEFORM



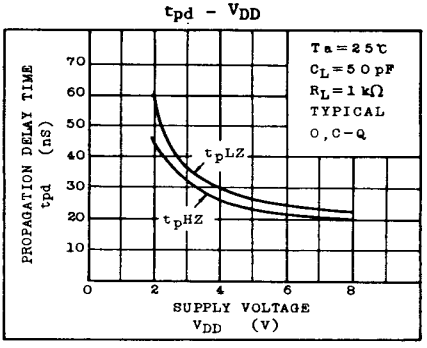
t_{pd} - V_{DD}



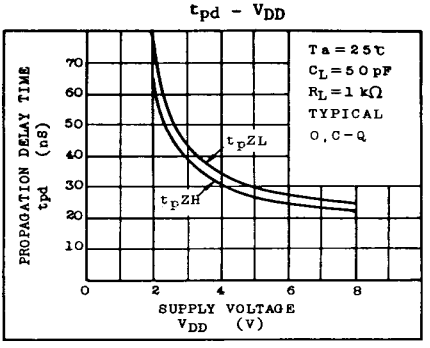
t_{pd} - C_L



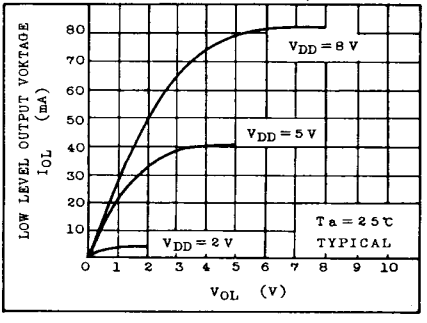
t_{pd} - V_{DD}



t_{pd} - V_{DD}



I_{OL} - V_{OL}



I_{OH} - (V_{DD} - V_{OH})