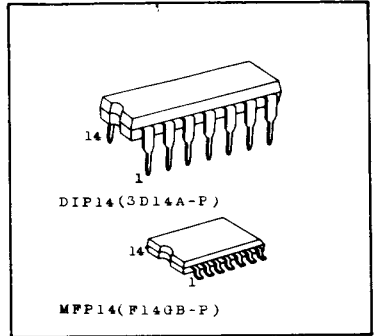
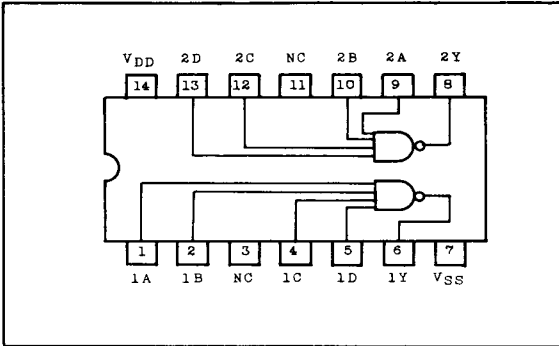


CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

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TC40H020 DUAL 4-INPUT NAND GATE

PIN CONNECTION



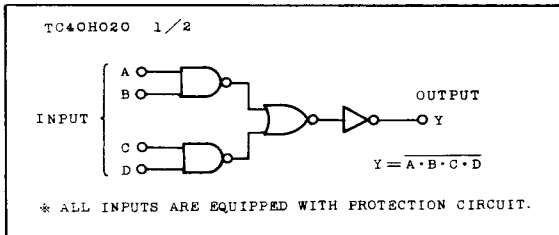
MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	$V_{SS}-0.5 \sim V_{SS}+10$	V
Input Voltage	V_{IN}	$V_{SS}-0.5 \sim V_{DD}+0.5$	V
Output Voltage	V_{OUT}	$V_{SS}-0.5 \sim V_{DD}+0.5$	V
Input Current	I_{IN}	± 10	mA
Power Dissipation	P_D	300(DIP)/180(MFP)	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	$^{\circ}\text{C}$
Lead Temp./Time	T_{sol}	$260^{\circ}\text{C} \cdot 10 \text{ sec}$	

TRUTH TABLE

INPUTS				OUTPUT
A	B	C	D	Y
L	L	L	L	H
H	L	L	L	H
L	H	L	L	H
H	H	L	L	H
L	L	H	L	H
H	L	H	L	H
L	H	H	L	H
H	H	H	L	H
L	L	L	H	H
H	L	L	H	H
L	H	L	H	H
H	H	L	H	H
L	L	H	H	H
H	L	H	H	H
L	H	H	H	H
H	H	H	H	L

LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS ($V_{SS}=0.0\text{V}$)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{DD}	-	2.0	-	8.0	V
Input Voltage	V_{IN}	-	0	-	V_{DD}	V
Operating Temperature	T_{opr}	-	-40	-	85	$^{\circ}\text{C}$

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ELECTRICAL CHARACTERISTICS (V_{SS}=0.0V)

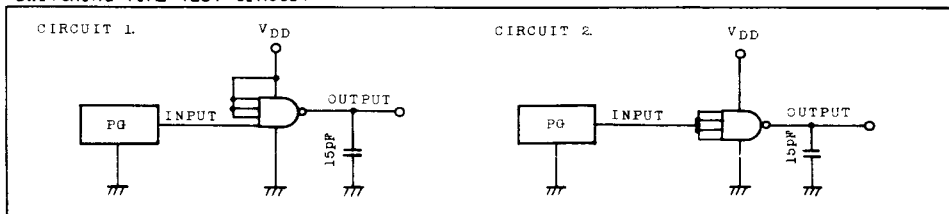
CHARACTERISTIC	SYMBOL	TEST CONDITION	V _{DD} (V)	-40°C		25°C			85°C		UNIT
				MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
High Level Output Voltage	V _{OH}	I _{OUT} < 1μA V _{IN} =V _{SS} , V _{DD}	5	4.95	-	4.95	5.0	-	4.95	-	V
Low Level Output Voltage	V _{OL}	I _{OUT} < 1μA V _{IN} =V _{DD}	5	-	0.05	-	0.0	0.05	-	0.05	
High Level Output Current	I _{OH}	V _{OH} =4.6V V _{IN} =V _{SS} , V _{DD}	5	-0.52	-	-0.44	-	-	-0.36	-	mA
Low Level Output Current	I _{OL}	V _{OL} =0.4V V _{IN} =V _{DD}	5	1.4	-	1.1	-	-	0.8	-	
Input Voltage	V _{IH} "H" Level	I _{OUT} < 1μA V _{OUT} =0.5V	5	4.0	-	4.0	-	-	4.0	-	V
	V _{IL} "L" Level		5	-	1.0	-	-	1.0	-	1.0	
Input Current	I _{IH} "H" Level	V _{IH} =8.0V	8	-	0.3	-	10 ⁻⁵	0.3	-	1.0	μA
	I _{IL} "L" Level	V _{IL} =0.0V	8	-	-0.3	-	10 ⁻⁵	-0.3	-	-1.0	
Quiescent Supply Current	I _{DD}	*V _{IN} =V _{SS} , V _{DD}	5	-	2.0	-	10 ⁻³	2.0	-	10.0	μA

* All valid input combinations.

SWITCHING CHARACTERISTICS (T_a=25°C, V_{SS}=0.0V, C_L=15pF)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V _{DD} (V)	MIN.	TYP.	MAX.	UNIT
Output Rise Time	t _{or}	Circuit 1	5	-	14	35	ns
Output Fall Time	t _{of}	Circuit 1	5	-	11	30	
Propagation Delay Time	t _{pLH} (Low-High)	Circuit 1	5	-	25	38	ns
Propagation Delay Time	t _{pHL} (High-Low)		5	-	20	30	
Propagation Delay Time	t _{pLH} (Low-High)	Circuit 2	5	-	20	30	
Propagation Delay Time	t _{pHL} (High-Low)		5	-	20	30	
Input Capacitance	C _{IN}			-	5	-	pF

SWITCHING TIME TEST CIRCUIT



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SWITCHING TIME TEST WAVEFORM

