

Data sheet acquired from Harris Semiconductor SCHS057A – Revised March 2002

CD4073B, CD4081B, CD4082B Types

CMOS AND Gates

High-Voltage Types (20-Volt Rating)

CD4073B Triple 3-Input AND Gate CD4081B Quad 2-Input AND Gate CD4082B Dual 4-Input AND Gate

CD4073B, CD4081B and CD4082B AND gates provide the system designer with direct implementation of the AND function and supplement the existing family of CMOS gates.

The CD4073B, CD4081B and CD4082B types are supplied in 14-lead dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic packages (E suffix), 14-lead small-outline package (NSR suffix), and in chip form (H suffix).

Features:

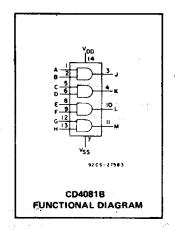
- Medium-Speed Operation -- tp_{LH}, tp_{HL} = 60 ns (typ.) at V_{DD} = 10 V
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (full package-temperature range) =

1 V at V_{DD} = 5 V

2 V at V_{DD} = 10 V

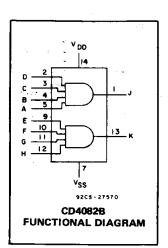
2.5 V at VDD = 15 V

- Standardized, symmetrical output characteristics
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Discription of 'B' Series CMOS Devices"



MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE FIANGE, (VDD)	
Voltages referenced to V _{SS} Terminal)0.5V to +2	20V
INPUT VOLTAGE RANGE, ALL INPUTS0.5V to VDD +0).5V
DC INPUT CURRENT, ANY ONE INPUT±10	
POWER DISSIPATION PER PACKAGE (Pp):	
For T _A = -55°C to +100°C 500r	nW
For TA = +1009C to +1259C	
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
FOR TA = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	nW
OPERATING-TEMPERATURE RANGE (T _A)55°C to +125°C	
STORAGE TEMPERATURE RANGE (T _{stg})65°C to +150°C)oC
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 \pm 1/32 inch (1.59 \pm 0.79mm) from case for 10s max+265	oC.



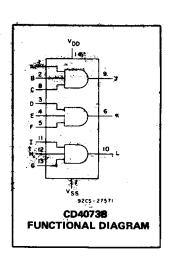
RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

OUA DA OTERIOTIO	LIN	4141174	
CHARACTERISTIC	MIN.	MAX.	UNITS
Supply-Voltage Range (For T _A = Full Package Temperature Range)	3	18	٧

DYNAMIC ELECTRICAL CHARACTERISTICS at TA=25°C, Input t_r,t_f=20 ns, and CL=50 pF, RL=200 k Ω

CHARACTE RÍSTIC	TEST COND	ITIONS	ALL T	LINUTO	
		V _{DD} Volts	TYP.	MAX.	UNITS
Propagation Delay Time,		5 10 15	125 60 45	250 120 90	ns
Transition Time, ^t THL ^{, t} TLH		5 10 15	100 50 40	200 100 80	ns
Input Capacitance, C _{IN}	Any Input	_	5	7.5	ρF



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STATIC ELECTRICAL CHARACTERISTICS

CHARACTER- ISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)								
	Vo	VIN	VDD	+25					UNITS			
	(v)	(V)	(V)	-56	-40	+85	+125	Min.	Тур.	Max.	-	
Quiescent Device Current, IDD Max.	1 111	0,5	5	0.25	0.25	7.5	7.5	_	0.01	0.25	μΑ	
	+.	0,10	10	0.5	0.5	15	15	_	0.01	0.5		
	-	0,15	15	1.	1	30	30	-	0,01	1		
		0,20	20	5	5	150	150	_	0.02	5		
Output Low (Sink) Current IOL Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	-	:	
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	-		
	1.5	0,15	15	4.2	4	2.8	2.4	34	6.8	_	1	
Output High (Source) Current, IOH Min.	4.6	0,5	5	-0.64	-0.61	-0.42	-0.36	-0.51	-1	-	mA ,	
	2.5	0,5	- 5	2	-1.8	-1.3	-1.15	-1.6	-3.2	_		
	9.5	0,10	10	1.6	-1.5	-1.1	-0.9	-1.3	-2.6	-		
	13.5	0,15	-15	-4.2	-4	-2.8	-2.4	-3.4	- 6.8	_		
Output Voltage:	-,	0,5	5		0	.05		-	0	0.05		
Low-Level,		0,10	10 ≡	0.05				0	0.05	,		
VOL Max		0,15	15	0.05			-	0	0.05	v		
Dutput Voltäge:		0,5	5	4.95				4.95	5	<u> </u>	"	
High-Level,		0,10	10		9	.95		9.95	10	-	1	
VOH Min.	* '	0,15	15	14.95 14.95 15				15	-			
Input Low	0.5	_	5	·	1	1.5			_	1.5		
Voltage;	1	. –	10			3		_	_	3	1	
VIE Max.	1.5	-	15			4		_	_	4	1	
Input High Voltage, VIH Min.	0.5,4.5	+	5	3.5			3.5	_	- I	٧		
	1,9	_	10	7			7		_			
	1.5,13.5	-	15			11		11	_	_		
Input Current ItN Max.		0,18	. 18	±0.1	±0.1	±1	±1	_	±10 ⁻⁵	±0.1	μΑ	

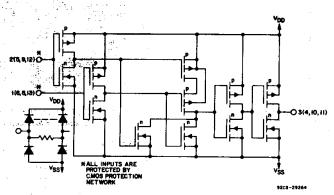


Fig. 1 - Schematic diagram for CD4081B (1 of 4 identical gates).

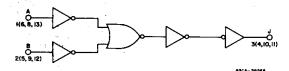


Fig. 2 - Logic diagram for CD4081B (1 of 4 identical gates).

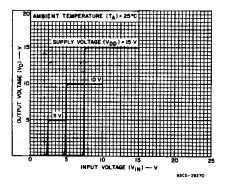


Fig. 3- Typical voltage transfer characteristics.

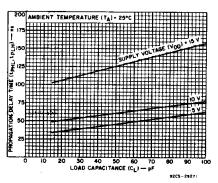


Fig. 4 — Typical propagation delay time as a function of load capacitance.

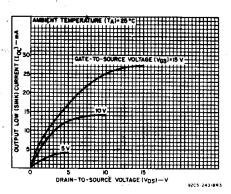


Fig. 5 — Typical output low (sink) current characteristics.

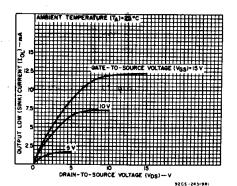


Fig. 6 — Minimum output low (sink) current characteristics.

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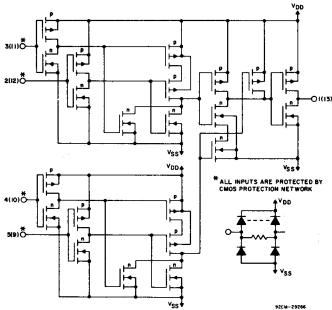


Fig. 7 - Schematic diagram for CD4082B (1 of 2 identical gates).

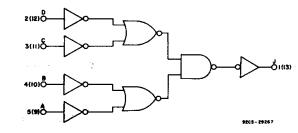


Fig. 9 - Logic diagram for CD4082B (1 of 2 identical gates).

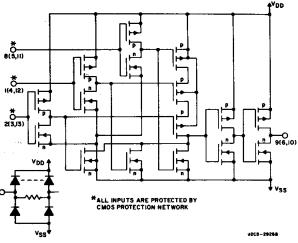


Fig. 11 — Schematic diagram for CD4073B (1 of 3 identical gates).

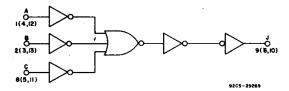


Fig. 13 — Logic diagram for CD4073B (1 of 3 identical gates).

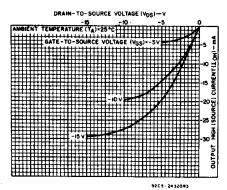


Fig. 8 - Typical output high (source) current characteristics.

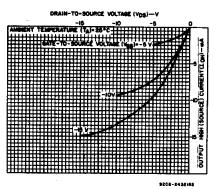


Fig. 10 — Minimum output high (source) current characteristics.

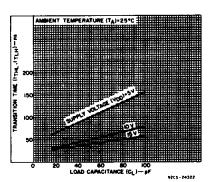


Fig. 12 — Typical transition time as a function of load capacitance

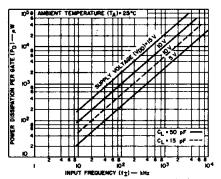


Fig. 14 — Typical dynamic power dissipation per gate as a function of frequency.

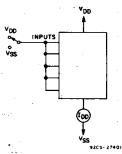


Fig. 15 - Quiescent device current test circuit.

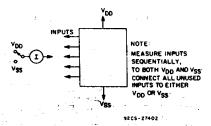


Fig. 16 - Input current test circuit.

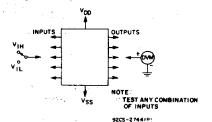
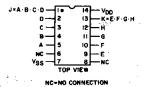


Fig. 17 - Input-voltage test circuit.

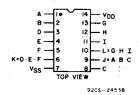
TERMINAL ASSIGNMENTS



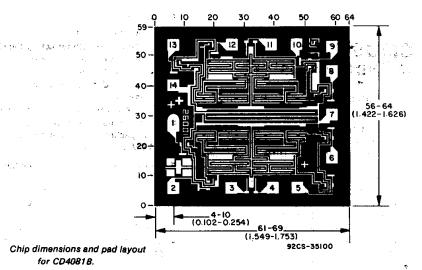
CD4081B

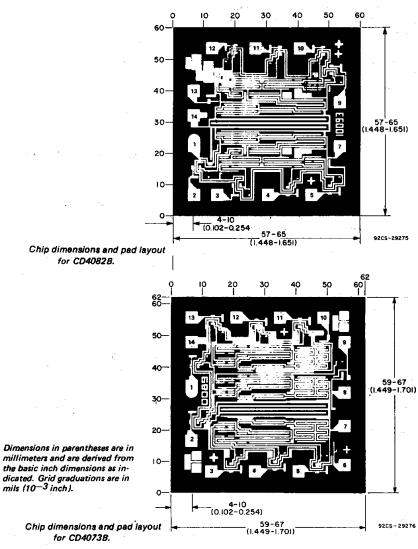


CD4082B



CD4073B





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