Data sheet acquired from Harris Semiconductor
SCHS015

CMOS NOR Gates

High-Voltage Types (20-Volt Rating)

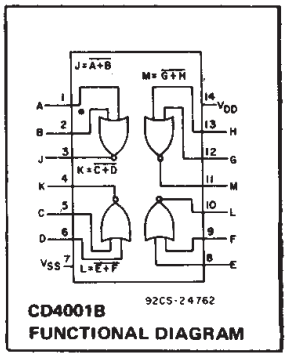
Quad 2 Input – CD4001B
Dual 4 Input – CD4002B
Triple 3 Input – CD4025B

■ CD4001B, CD4002B, and CD4025B NOR gates provide the system designer with direct implementation of the NOR function and supplement the existing family of CMOS gates. All inputs and outputs are buffered.

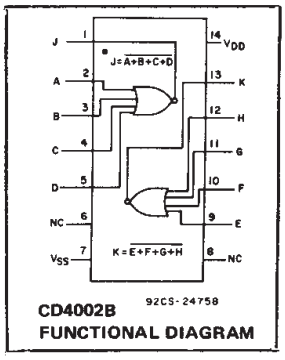
The CD4001B, CD4002B, and CD4025B types are supplied in 14-lead hermetic dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic packages (E suffix), and in chip form (H suffix).

Features:

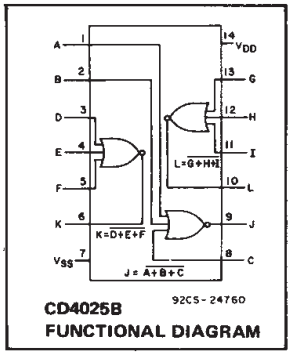
- Propagation delay time = 60 ns (typ.) at C_L = 50 pF, V_{DD} = 10 V
- Buffered inputs and outputs
- Standardized symmetrical output characteristics
- 100% tested for maximum quiescent current at 20 V
- 5-V, 10-V, and 15-V parametric ratings
- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (over full package temperature range):
  1 V at V_{DD} = 5 V
  2 V at V_{DD} = 10 V
  2.5 V at V_{DD} = 15 V
- Meets all requirements of JEDEC Tentative **Standard No. 13B, "Standard Specifications** for Description of "B" Series CMOS Devices"



CD4001B
FUNCTIONAL DIAGRAM



CD4002B
FUNCTIONAL DIAGRAM



CD4025B
FUNCTIONAL DIAGRAM

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
								+25			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	0.25	0.25	7.5	7.5	–	0.01	0.25	μA
	–	0,10	10	0.5	0.5	15	15	–	0.01	0.5	
	–	0,15	15	1	1	30	30	–	0.01	1	
	–	0,20	20	5	5	150	150	–	0.02	5	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5,4.5	–	5	1.5				—	—	1.5	V
	1,9	–	10	3				—	—	3	
	1.5,13.5	–	15	4				—	—	4	
Input High Voltage, V_{IH} Min.	0.5	–	5	3.5				3.5	—	—	
	1	–	10	7				7	—	—	
	1.5	–	15	11				11	—	—	
Input Current I_{IN} Max.		0,18	18	±0.1	±0.1	±1	±1	–	$\pm 10^{-5}$	±0.1	μA

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package Temperature Range)	3	18	V

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
Voltages referenced to V_{SS} Terminal) ..... -0.5V to +20V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5V to V_{DD} +0.5V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55°C to +100°C 500mW
For T_A = +100°C to +125°C ..... Derate Linearity at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) 100mW
OPERATING-TEMPERATURE RANGE (T_A) ..... -55°C to +125°C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... -65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max ..... +265°C

DYNAMIC ELECTRICAL CHARACTERISTICS

At T_A = 25°C; Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200kΩ

CHARACTERISTIC	TEST CONDITIONS	ALL TYPES LIMITS			UNITS
		V_{DD} VOLTS	TYP.	MAX.	
Propagation Delay Time, t_{PHL}, t_{PLH}		5	125	250	ns
		10	60	120	
		15	45	90	
Transition Time, t_{THL}, t_{TLH}		5	100	200	ns
		10	50	100	
		15	40	80	
Input Capacitance, C_{IN}	Any Input		5	7.5	pF

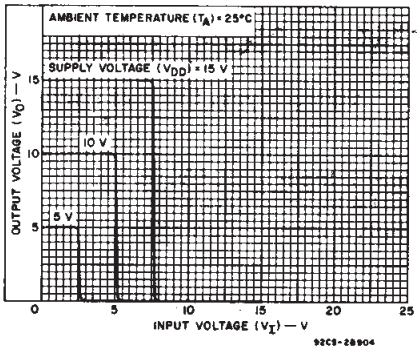


Fig.1 – Typical voltage transfer characteristics.

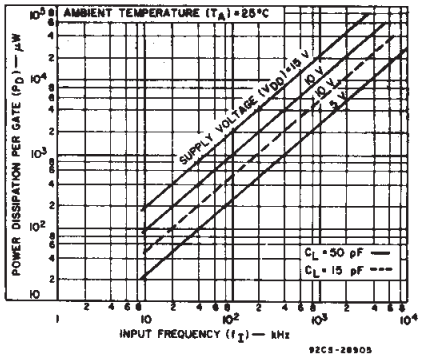


Fig.2 – Typical power dissipation vs. frequency.

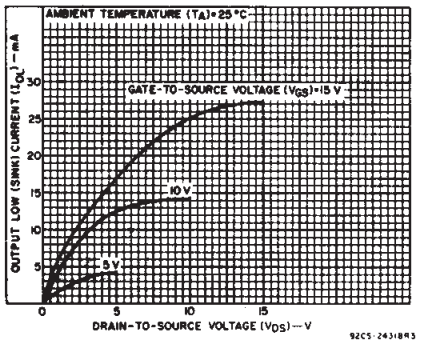


Fig.3 – Typical output low (sink) current characteristics.

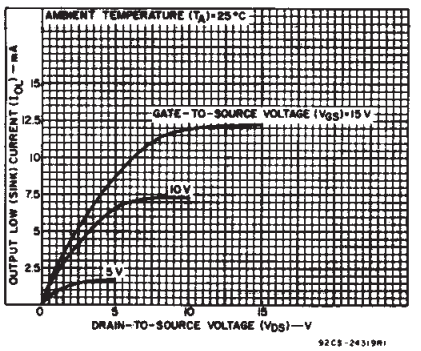


Fig. 4 – Minimum output low (sink) current characteristics.

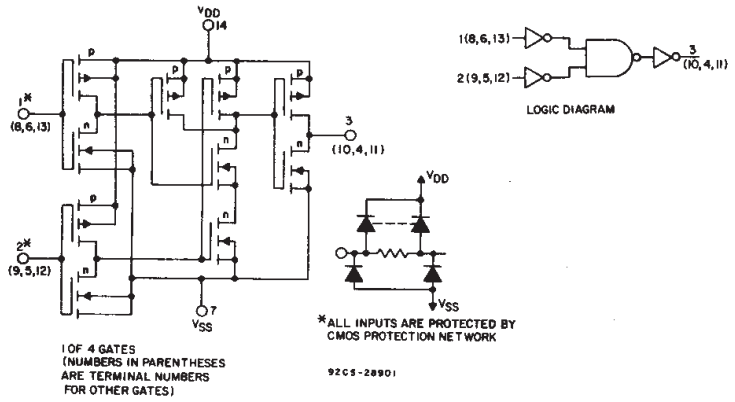


Fig.5 – Schematic and logic diagrams for CD4001B.

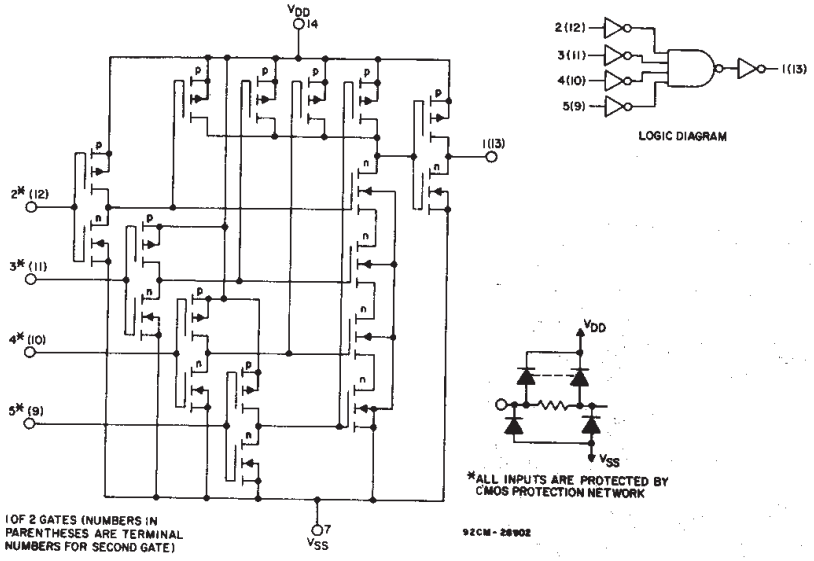


Fig. 6 – Schematic and logic diagrams for CD4002B.

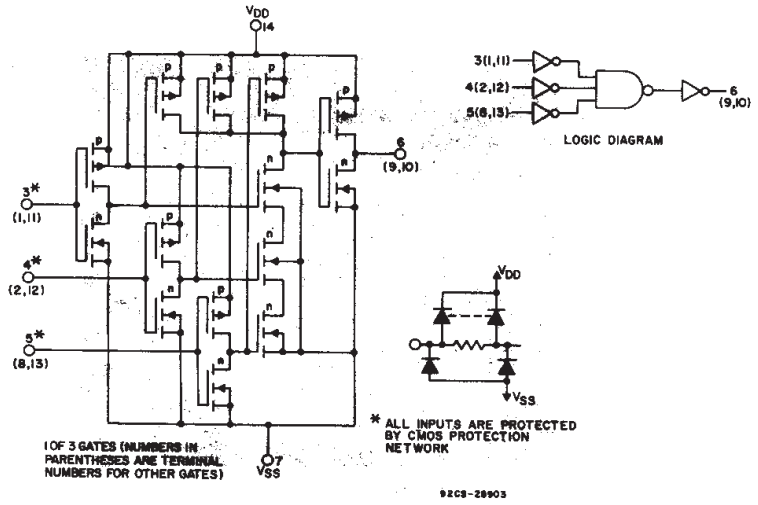


Fig. 7 – Schematic and logic diagrams for CD4025B.

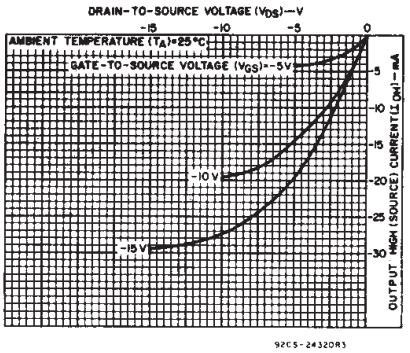


Fig. 8 – Typical output high (source) current characteristics.

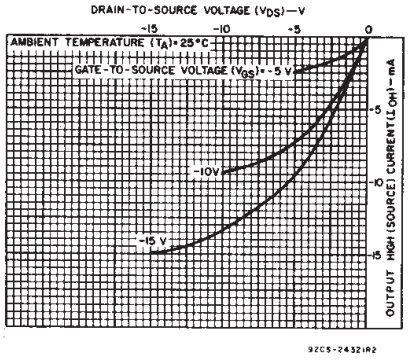


Fig. 9 – Minimum output high (source) current characteristics.

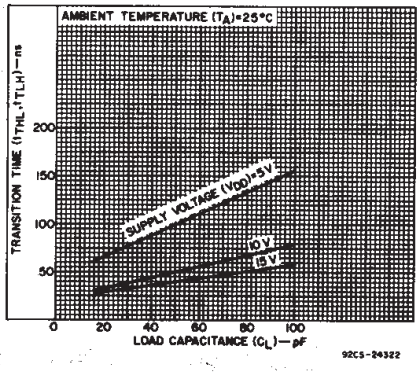


Fig. 10 – Typical transition time vs. load capacitance.

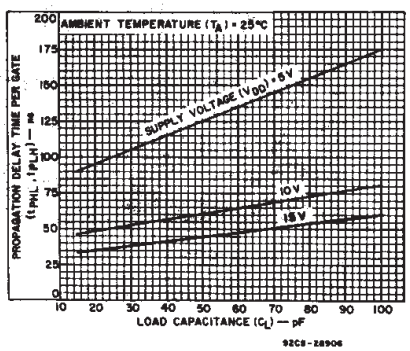


Fig. 11 – Typical propagation delay time vs. load capacitance.

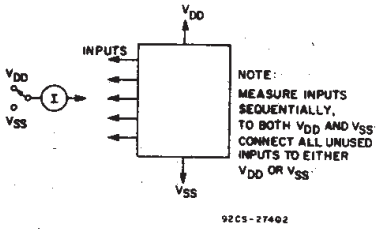


Fig. 13 – Input leakage current test circuit.

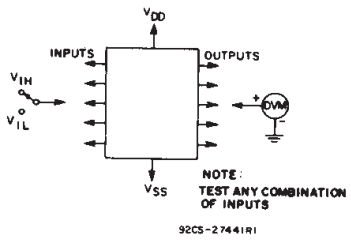


Fig. 14 – Input-voltage test circuit.

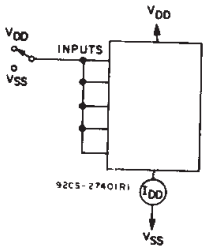
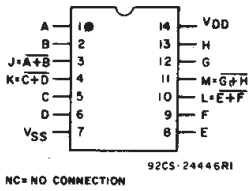
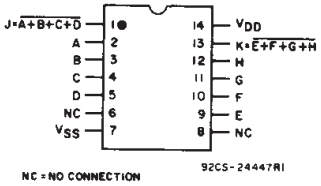


Fig. 15 – Quiescent-device current test circuit.

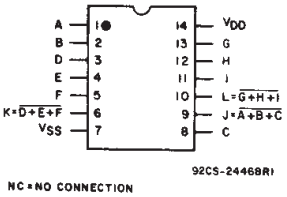
TERMINAL ASSIGNMENTS (TOP VIEW)



CD4001B

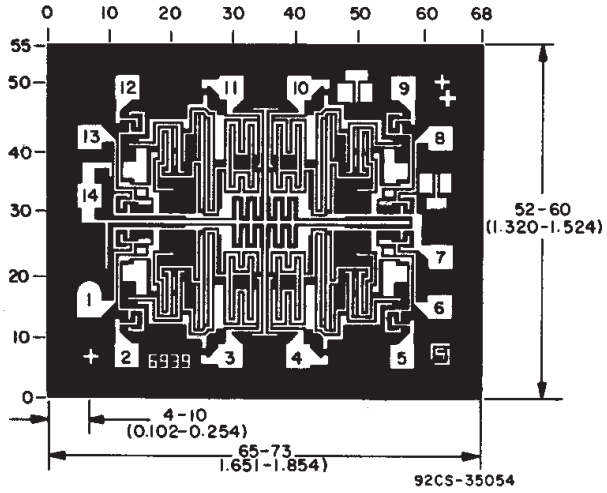


CD4002B

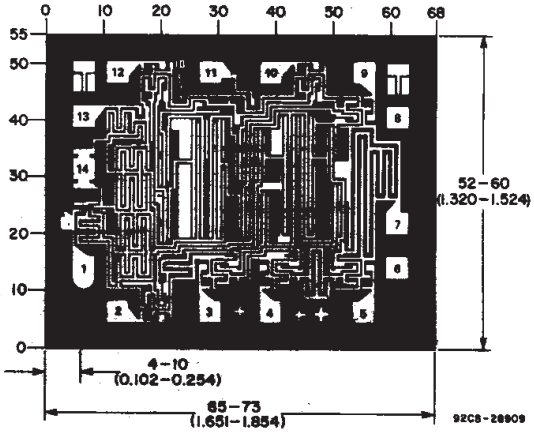


CD4025B

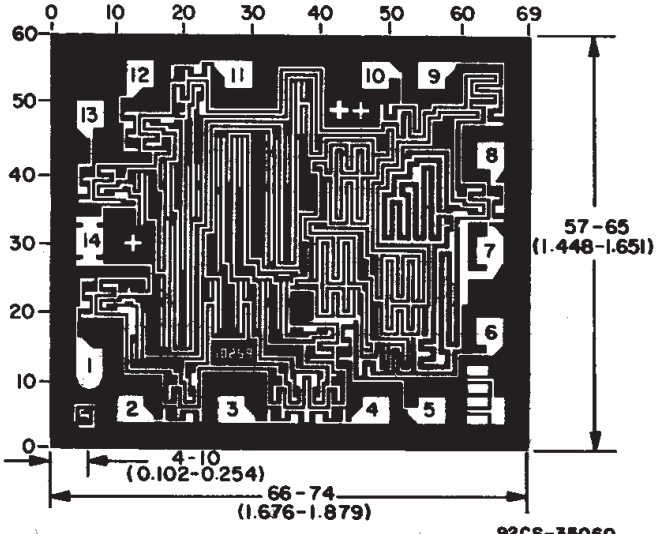
Chip Dimensions and Pad Layouts



CD4001B



CD4002B



CD4025B

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CD4001B, CMOS Quad 2-Input NOR Gate

Device Status: Active

Parameter Name	CD4001B
Voltage Nodes (V)	5, 10, 15

Description

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- Meets all requirments of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

To view the following documents, Acrobat Reader 3.x is required.
To download a document to your hard drive, right-click on the link and choose 'Save'.

Datasheets

Full datasheet in Acrobat PDF: schs015.pdf (206 KB)
Full datasheet in Zipped PostScript: schs015.psz (349 KB)

Pricing/Samples/Availability

Orderable Device	Package	Pins	Temp (°C)	Status	Price/unit USD (100-999)	Pack Qty	DSCC Number	Availability / Samples
89263AKB3T	WR	16	-55 TO 125	OBSOLETE				
CD4001BE	N	14	-55 TO 125	ACTIVE	0.28	25		Check stock or order
CD4001BF	J	14	-55 TO 125	ACTIVE	2.44	1		Check stock or order
CD4001BF3A	J	14	-55 TO 125	ACTIVE	2.87	1		Check stock or order

CD4001BM	D	14	-55 TO 125	ACTIVE	0.34	50		Check stock or order
CD4001BM96	D	14	-55 TO 125	ACTIVE	0.36	2500		Check stock or order
CD4001BNSR	NS	14	-55 TO 125	ACTIVE	0.38	2000		Check stock or order
CD4001BPW	PW	14	-55 TO 125	OBSOLETE				
CD4001BPWR	PW	14	-55 TO 125	ACTIVE	0.30	2000		Check stock or order
JM38510/05252BCA	J	14	-55 TO 125	ACTIVE	14.61	1		Check stock or order

Application Reports

View Application Reports for Digital Logic

Related Documents

- Documentation Rules (SAP) And Ordering Information (SZZU001B, 4 KB - Updated: 05/06/1999)
- Logic Selection Guide Second Half 2000 (SDYU001N, 5035 KB - Updated: 04/17/2000)
- MicroStar Junior BGA Design Summary (SCET004, 284 KB - Updated: 07/28/2000)
- More Power In Less Space - Technical Article (SCAU001A, 850 KB - Updated: 03/01/1996)

Table Data Updated on: 8/30/2000